Technical Information

PALMiCE2 / PALMiCE3
SuperH-related Target Interface

Feb. 22, 2013
Tenth Edition

Go through the required procedures as stated under Foreign Exchange and Foreign Trade Control Law in exporting (including the case where travellers directly carry) this product or providing this product for residents outside Japan.

Document change history

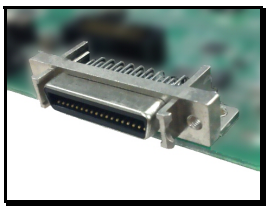
First Edition	Feb. 12, 2008	Initial edition
Second Edition	Dec. 12, 2008	**Added a package to the table of Signals.** SH7750R SH7751R
Third Edition	Jun. 30, 2009	**CSIDE for PALMiCE3-SH-E (Ver.5.10.00) was released.** ・ **Added PALMiCE3 to Applicable products for the following CPUs.** SH7047F SH7083F/SH7084F/SH7085F/SH7086F SH7144F/SH7145F SH7606 SH7618 SH7615 SH7616 SH7206 SH7705 SH7706 SH7709S SH7710 SH7712 SH7720 SH7727 SH7729 SH7729R SH7750R/SH7750S SH7751/SH7751R SH7760 SH7780 ・ **Added the following CPUs to this manual.** SH7146F SH7149F SH7618A SH7211F SH7243F/SH7285F/ SH7286F SH7201 SH7203 SH7261 SH7262/SH7264 SH7263 SH7670/SH7671/SH7672/SH7673 SH7205 SH7265 SH7290(SH-Mobile3AS) SH7294(SH-MobileJ) SH7300(SH-MobileV) SH7713 SH7721 SH7343(SH-Mobile3AS) SH7354(SH-MobileL3V) SH7722(SH-MobileR) SH7723(SH-MobileR2) SH7730 SH7763 SH7764 SH7770 SH7774 SH7780 SH7781 SH7785 **CSIDE for PALMiCE3 SH7055-E (Ver.5.07.00) was released.** ・ **Added the following CPUs to this manual.** SH7055F SH7055SF SH7058F SH7058SF/SH7059F **Changed the descriptions of AUDSYNC signal regarding the following CPUs.** They had been written in negative logic, however, the descriptions were changed to positive logic so that they conform to the descriptions in the hardware manual published by Renesas Technology Corp.. SH7705 SH7751/SH7751R SH7760 SH7780

Fourth Edition	Sep. 30, 2009	**SH7243F/SH7285F/ SH7286F** Edited the note on MDR connector.
Fifth Edition	Jun. 1, 2010	・ **Made provision of support for Mictor connector.** SH7206 SH7211F SH7243F/SH7285F/SH7286F SH7201 SH7203 SH7261 SH7262/SH7264 SH7263 SH7205 SH7265 SH7723(SH-MobileR2) SH7730 SH7764 ・ **SH7201, SH7261** Added the note on MDR connector. ・ **SH7785** Edited the contents of note *3 and *4 of Mictor connector signal table.
Sixth Edition	Aug. 2, 2010	・ **SH7243F/SH7285F/SH7286F** The note on the use of PALMiCE3-SH AUD360 model given for MDR connector will now apply to all connectors. ・ **Added the note on the use of PALMiCE3-SH AUD360 model.** SH7083F/SH7084F/SH7085F/SH7086F SH7146F SH7149F
Seventh Edition	Apr. 01, 2011	・ **Added pages for description of the following:** PALMiCE3 - Supported connectors PALMiCE3 - Target probe specifications
Eighth Edition	Jul. 12, 2011	・ **Changed the format.**
Ninth Edition	Apr. 11, 2012	・ **Corrected the product name listed for Mictor probe under PALMiCE3 - Target probe specifications as it contained errors.** [Correct] P3-SH-PRB-MIC38-MIC38 [Incorrect] P3-RE-PRB-MIC38-MIC38
Tenth Edition	Feb. 22, 2013	・ **PALMiCE3 - Supported connectors** Added the pin configuration and note.

PALMiCE3 - Supported connectors

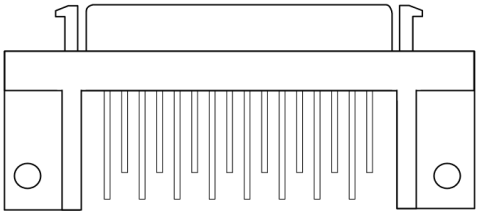
(For detailed dimensions of the connectors, refer to the documentations by respective manufacturers of the connectors.)

36-pin MDR connector

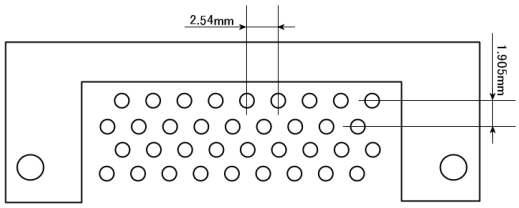


Recommended connector
Manufacturer : 3M
Model : 10236-52A2JL

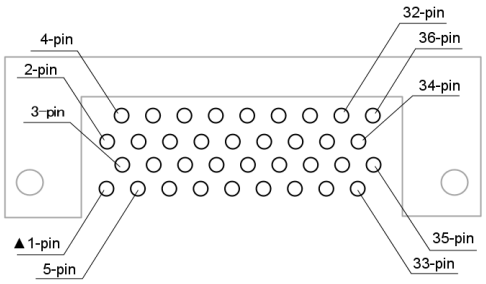
●Top view on the target board



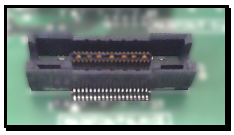
●Side view on the target board



●Pin configuration

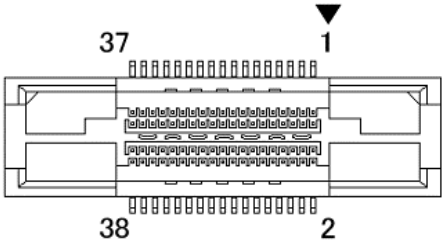


38-pin Mictor connector



Recommended connector
Manufacturer : AMP
Model : Mictor connector
2-767004-2 / 767054-1 / 767061

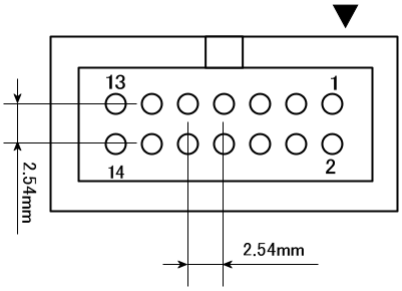
●Top view on the target board and Pin configuration



14-pin MIL connector

Recommended connector
Manufacturer : Omron Corporation
Model : XG4C-1431

●Top view on the target board and Pin configuration



*** Please look at the pin configuration diagram and make sure that the connector is in the right direction before connecting.**

Moreover, please check the pin number in the corresponding signal table and make sure the signal and the pin numbers match.

PALMiCE3 - Target probe specifications

Connector to be mounted on the target board		Required target probe
36-pin MDR connector	→	AUD probe
38-pin Mictor connector	→	Mictor probe
14-pin MIL connector	→	HUDI cable

Target probe specifications

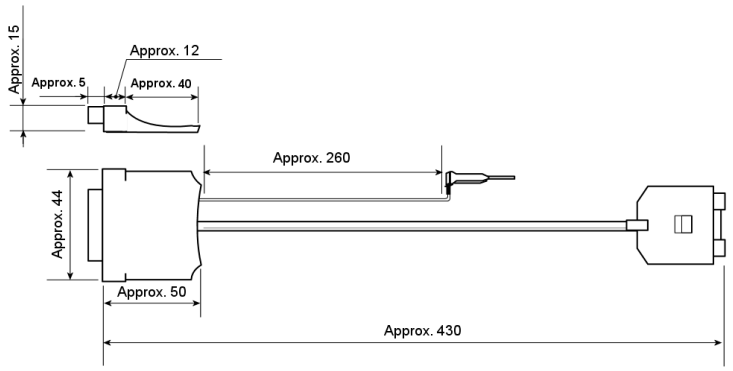
To be used by connecting it to PALMiCE3 main unit.

target system — Target probe — PALMiCE3

AUD probe

Product : P3-SH-PRB-MIC38-MDR36

Probe for connecting PALMiCE3 AUD360 main unit to 36-pin MDR connector on the target system.

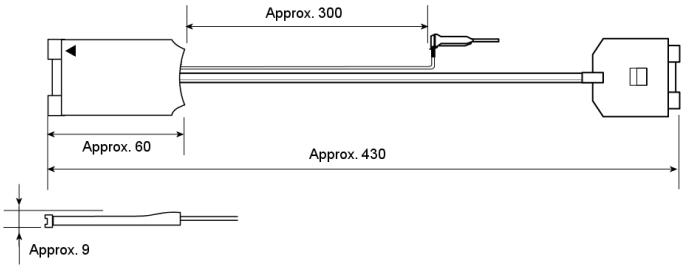


(Unit: mm)

Mictor probe

Product : P3-SH-PRB-MIC38-MIC38

Probe for connecting PALMiCE3 AUD360 main unit to 38-pin Mictor connector on the target system.

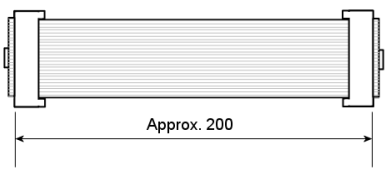


(Unit: mm)

HUDI cable

Product : P3-CB-MIL14-MIL14

Probe for connecting PALMiCE3 HUDI141 main unit to 14-pin MIL connector on the target system.



(Unit: mm)

SH-2

SH7047F
SH7055F
SH7055SF
SH7058F
SH7058SF/SH7059F
SH7083F/SH7084F/SH7085F/SH7086F
SH7144F/SH7145F
SH7146F
SH7149F
SH7606
SH7618/SH7618A
SH7619

SH7047F

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP-100	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP-100
1	TCK	Input	63	2	N.C.		
3	$\overline{\text{TRST}}$	Input	58	4	GND($\overline{\text{DBGMD}}$)*2	(Input)	(16)
5	TDO	Output	60	6	GND		
7	$\overline{\text{ASEBRKAK}}$	Output	11	8	VCC *3	Output	
9	TMS	Input	59	10	GND		
11	TDI	Input	61	12	GND		
13	$\overline{\text{RES}}$	Output	87	14	GND		

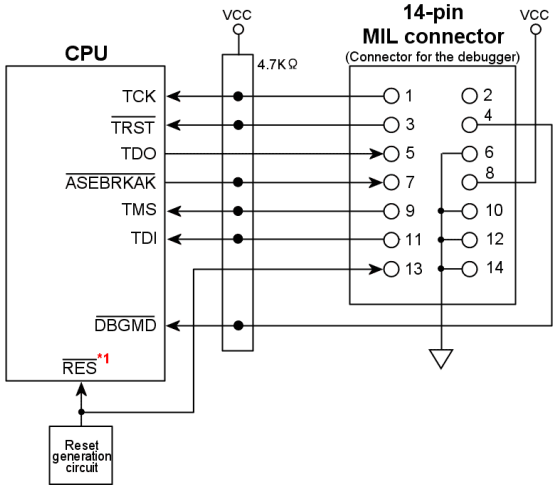
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{DBGMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{DBGMD}}$ pin to Low state when you connect $\overline{\text{DBGMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{DBGMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{DBGMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{DBGMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

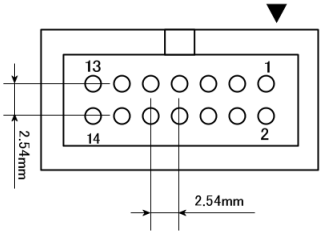
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP-100	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP-100
1	AUDCK	Input/Output	79	2	GND		
3	AUDATA0	Input/Output	92	4	GND		
5	AUDATA1	Input/Output	90	6	GND		
7	AUDATA2	Input/Output	88	8	GND		
9	AUDATA3	Input/Output	86	10	GND		
11	$\overline{\text{AUDSYNC}}$	Input/Output	78	12	GND		
13	$\overline{\text{AUDRST}}$	Input	81	14	GND		
15	AUDMD	Input	80	16	GND		
17	TCK	Input	63	18	GND		
19	TMS	Input	59	20	GND		
21	$\overline{\text{TRST}}$	Input	58	22	GND($\overline{\text{DBGMD}}$)*2	(Input)	(16)
23	TDI	Input	61	24	GND		
25	TDO	Output	60	26	GND		
27	$\overline{\text{ASEBRKAK}}$	Output	11	28	GND		
29	VCC*3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	87	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

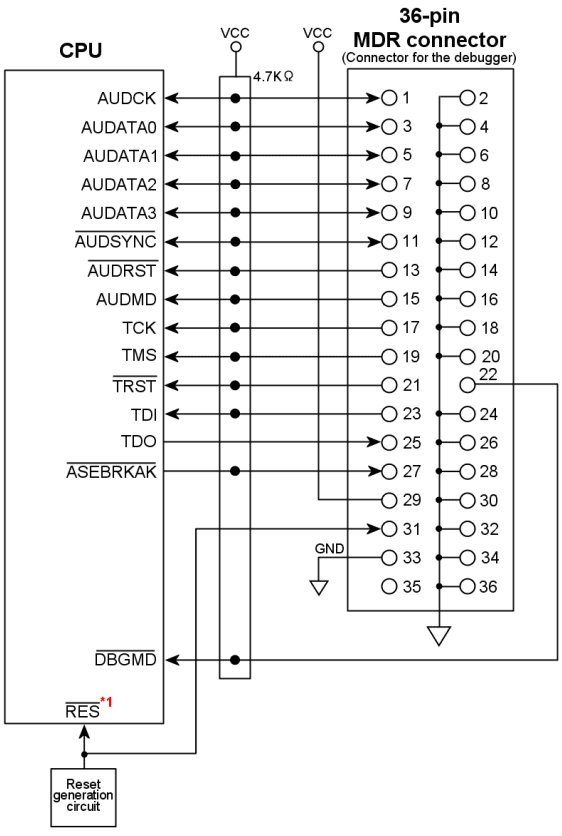
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{DBGMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{DBGMD}}$ pin to Low state when you connect $\overline{\text{DBGMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{DBGMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{DBGMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{DBGMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

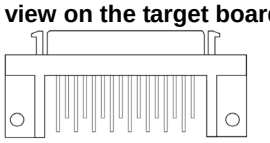
Target connection reference diagram



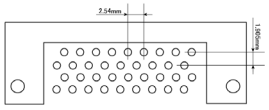
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

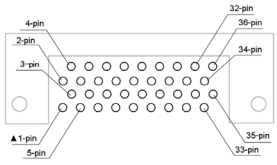
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7047F)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7055F

Applicable product	PALMiCE3-SH7055
Applicable connector (Connector for debugger)	MDR connector (36-pin design)

MDR connector

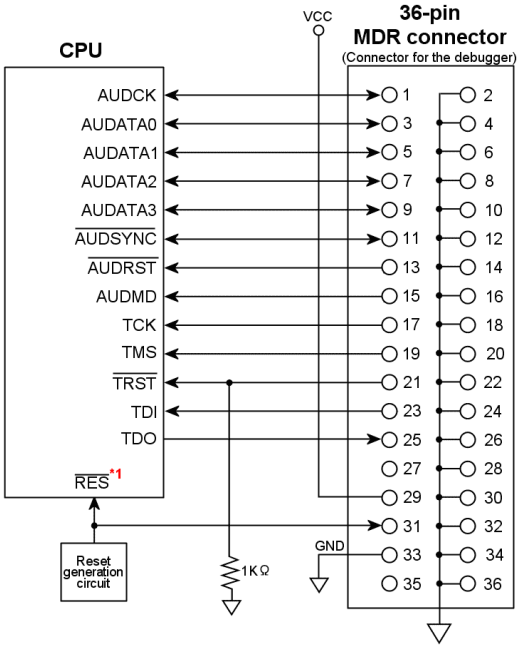
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-256H	Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-256H
1	AUDCK	Input/Output	245	2	GND		
3	AUDATA0	Input/Output	241	4	GND		
5	AUDATA1	Input/Output	242	6	GND		
7	AUDATA2	Input/Output	243	8	GND		
9	AUDATA3	Input/Output	244	10	GND		
11	$\overline{\text{AUDSYNC}}$	Input/Output	246	12	GND		
13	$\overline{\text{AUDRST}}$	Input	238	14	GND		
15	AUDMD	Input	240	16	GND		
17	TCK	Input	236	18	GND		
19	TMS	Input	232	20	GND		
21	$\overline{\text{TRST}}$	Input	233	22	GND		
23	TDI	Input	234	24	GND		
25	TDO	Output	235	26	GND		
27	N.C.			28	GND		
29	VCC *2	Output		30	GND		
31	$\overline{\text{RES}}$	Output	58	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

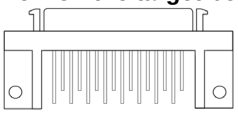
Target connection reference diagram



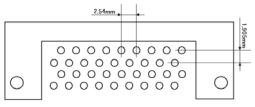
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

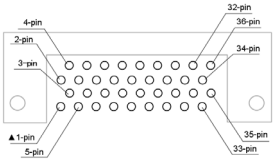
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7055F)

First Edition	Jun. 30, 2009	Initial edition

SH7055SF

Applicable product	PALMiCE3-SH7055
Applicable connector (Connector for debugger)	MDR connector (36-pin design)

MDR connector

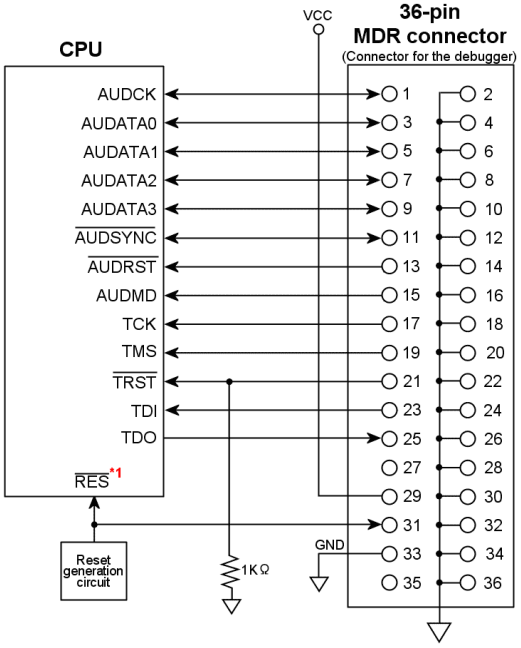
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-256H	Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-256H
1	AUDCK	Input/Output	245	2	GND		
3	AUDATA0	Input/Output	241	4	GND		
5	AUDATA1	Input/Output	242	6	GND		
7	AUDATA2	Input/Output	243	8	GND		
9	AUDATA3	Input/Output	244	10	GND		
11	$\overline{\text{AUDSYNC}}$	Input/Output	246	12	GND		
13	$\overline{\text{AUDRST}}$	Input	238	14	GND		
15	AUDMD	Input	240	16	GND		
17	TCK	Input	236	18	GND		
19	TMS	Input	232	20	GND		
21	$\overline{\text{TRST}}$	Input	233	22	GND		
23	TDI	Input	234	24	GND		
25	TDO	Output	235	26	GND		
27	N.C.			28	GND		
29	VCC *2	Output		30	GND		
31	$\overline{\text{RES}}$	Output	58	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

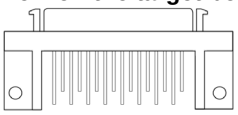
Target connection reference diagram



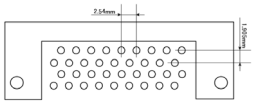
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

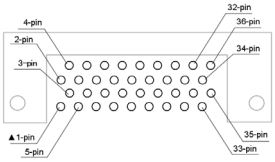
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7055SF)

First Edition	Jun. 30, 2009	Initial edition

SH7058F

Applicable product	PALMiCE3-SH7055
Applicable connector (Connector for debugger)	MDR connector (36-pin design)

MDR connector

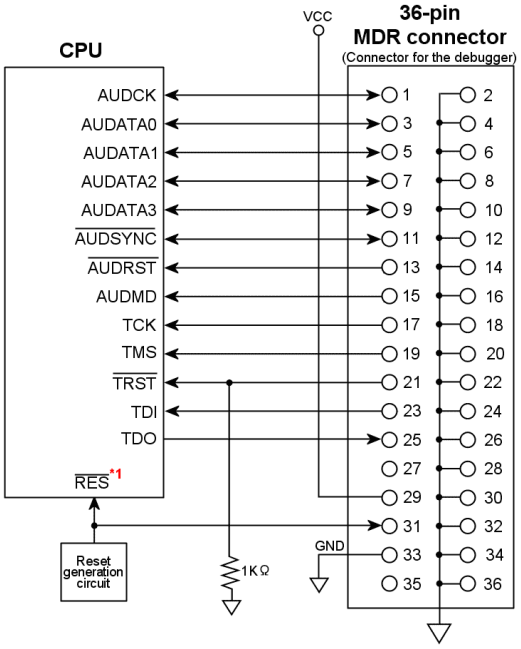
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-256H	BP-272				FP-256H	BP-272
1	AUDCK	Input/Output	245	D1	2	GND			
3	AUDATA0	Input/Output	241	G1	4	GND			
5	AUDATA1	Input/Output	242	F1	6	GND			
7	AUDATA2	Input/Output	243	G2	8	GND			
9	AUDATA3	Input/Output	244	E1	10	GND			
11	$\overline{\text{AUDSYNC}}$	Input/Output	246	F2	12	GND			
13	$\overline{\text{AUDRST}}$	Input	238	H2	14	GND			
15	AUDMD	Input	240	H3	16	GND			
17	TCK	Input	236	J2	18	GND			
19	TMS	Input	232	K3	20	GND			
21	$\overline{\text{TRST}}$	Input	233	J1	22	GND			
23	TDI	Input	234	K4	24	GND			
25	TDO	Output	235	H1	26	GND			
27	N.C.				28	GND			
29	VCC *2	Output			30	GND			
31	$\overline{\text{RES}}$	Output	58	B16	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

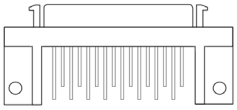
Target connection reference diagram



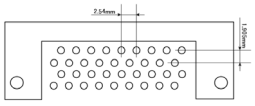
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

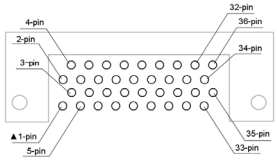
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7058F)

First Edition	Jun. 30, 2009	Initial edition

SH7058SF/SH7059F

Applicable product	PALMiCE3-SH7055
Applicable connector (Connector for debugger)	MDR connector (36-pin design)

MDR connector

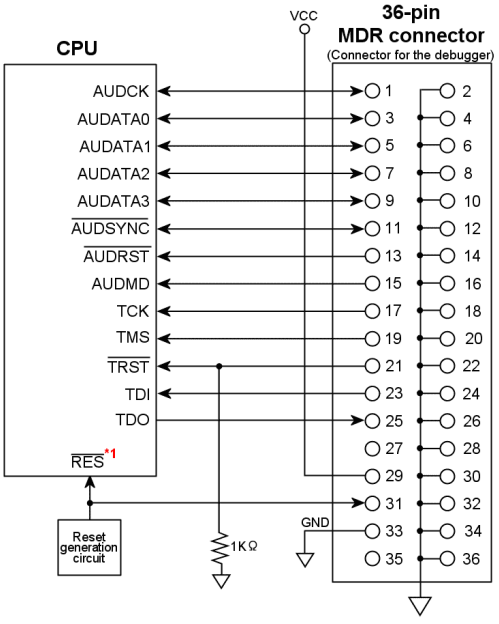
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-256H	BP-272				FP-256H	BP-272
1	AUDCK	Input/ Output	245	D1	2	GND			
3	AUDATA0	Input/ Output	241	G1	4	GND			
5	AUDATA1	Input/ Output	242	F1	6	GND			
7	AUDATA2	Input/ Output	243	G2	8	GND			
9	AUDATA3	Input/ Output	244	E1	10	GND			
11	$\overline{\text{AUDSYNC}}$	Input/ Output	246	F2	12	GND			
13	$\overline{\text{AUDRST}}$	Input	238	H2	14	GND			
15	AUDMD	Input	240	H3	16	GND			
17	TCK	Input	236	J2	18	GND			
19	TMS	Input	232	K3	20	GND			
21	$\overline{\text{TRST}}$	Input	233	J1	22	GND			
23	TDI	Input	234	K4	24	GND			
25	TDO	Output	235	H1	26	GND			
27	N.C.				28	GND			
29	VCC *2	Output			30	GND			
31	$\overline{\text{RES}}$	Output	58	B16	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

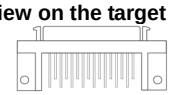
Target connection reference diagram



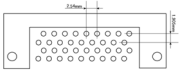
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

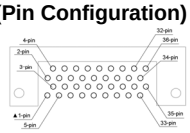
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$pin of CPU.

Document change history (SH7058SF/SH7059F)

First Edition	Jun. 30, 2009	Initial edition

SH7083F/SH7084F/SH7085F/SH7086F

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

NB : When you use PALMiCE3-SH AUD360 model and if you are using CPU with voltage over 4.0V, please contact us.

MIL connector

Signals

Pin No.	Signal	Input/ Output *1	CPU Pin No. 7083F TQFP-100	7083F P-LBGA-112	7084F LQFP-112	7085F LQFP-144	7086F LQFP-176	Pin No.	Signal	Input/ Output *1	CPU Pin No. 7083F TQFP-100	7083F P-LBGA-112	7084F LQFP-112	7085F LQFP-144	7086F LQFP-176
1	TCK	Input	80	A9	89	143	1	2	N.C.						
3	$\overline{\text{TRST}}$	Input	77	A10	86	139	174	4	GND ($\overline{\text{ASEMD0}}$) *2	(Input)	(27)	(L2)	(33)	(42)	(51)
5	TDO	Output	79	B9	88	142	176	6	GND						
7	$\overline{\text{ASEBRKAK}}$ / $\overline{\text{ASEBRK}}$	Input/ Output	100	A2	102	144	2	8	VCC *3	Output					
9	TMS	Input	76	B10	85	138	172	10	GND						
11	TDI	Input	78	D8	87	140	175	12	GND						
13	$\overline{\text{RES}}$	Output	75	C9	84	108	132	14	GND						

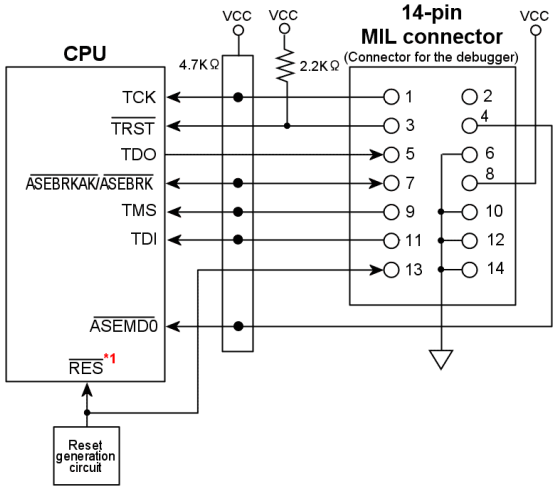
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: $\overline{\text{ASEMD0}}$To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

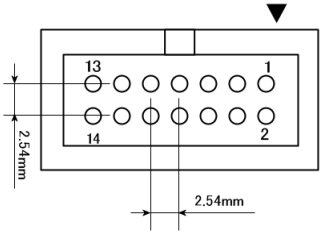
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

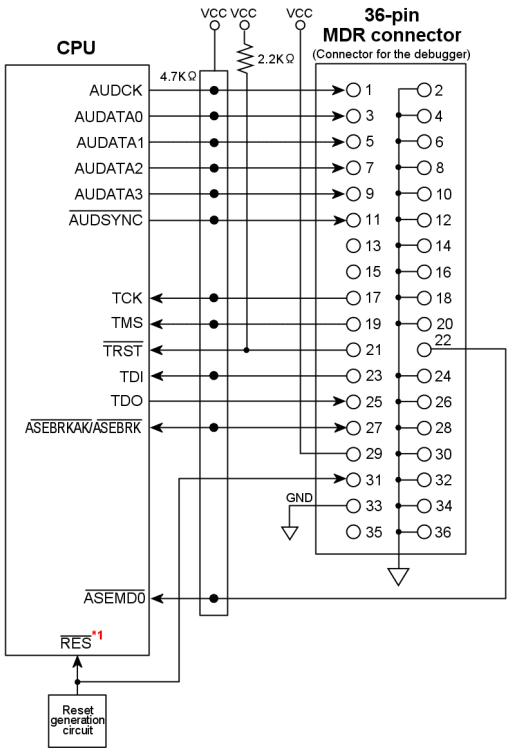
Signals

Pin No.	Signal	Input/ Output *1	CPU Pin No. 7083F TQFP-100	7083F P-LBGA-112	7084F LQFP-112	7085F *2 LQFP-144	7086F *2 LQFP-176	Pin No.	Signal	Input/ Output *1	CPU Pin No. 7083F TQFP-100	7083F P-LBGA-112	7084F LQFP-112	7085F *2 LQFP-144	7086F *2 LQFP-176
1	AUDCK	Output	45	H7	53	65/109	89/133	2	GND						
3	AUDATA0	Output	51	K10	60	72/116	97/140	4	GND						
5	AUDATA1	Output	50	L10	59	70/115	95/139	6	GND						
7	AUDATA2	Output	49	K9	58	69/114	93/138	8	GND						
9	AUDATA3	Output	48	J8	57	68/113	92/137	10	GND						
11	$\overline{\text{AUDSYNC}}$	Output	44	L8	52	64/100	88/124	12	GND						
13	N.C.							14	GND						
15	N.C.							16	GND						
17	TCK	Input	80	A9	89	143	1	18	GND						
19	TMS	Input	76	B10	85	138	172	20	GND						
21	$\overline{\text{TRST}}$	Input	77	A10	86	139	174	22	GND ($\overline{\text{ASEMD0}}$)*3	(Input)	(27)	(L2)	(33)	(42)	(51)
23	TDI	Input	78	D8	87	140	175	24	GND						
25	TDO	Output	79	B9	88	142	176	26	GND						
27	$\overline{\text{ASEBRKAK}}$ / $\overline{\text{ASEBRK}}$	Input/ Output	100	A2	102	144	2	28	GND						
29	VCC*4	Output						30	GND						
31	$\overline{\text{RES}}$	Output	75	C9	84	108	132	32	GND						
33	GND							34	GND						
35	N.C.							36	GND						

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For SH7085F and SH7086F respectively, 2 routings of AUD ports are available. Choose either of the routings.
*3: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*4: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

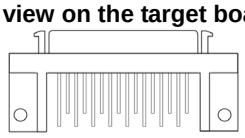
Target connection reference diagram



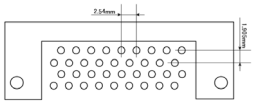
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

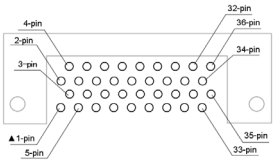
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7083F/SH7084F/SH7085F/SH7086F)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.
Third Edition	Aug. 2, 2010	Added the note on the use of PALMiCE3-SH AUD360 model.

SH7144F/SH7145F

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

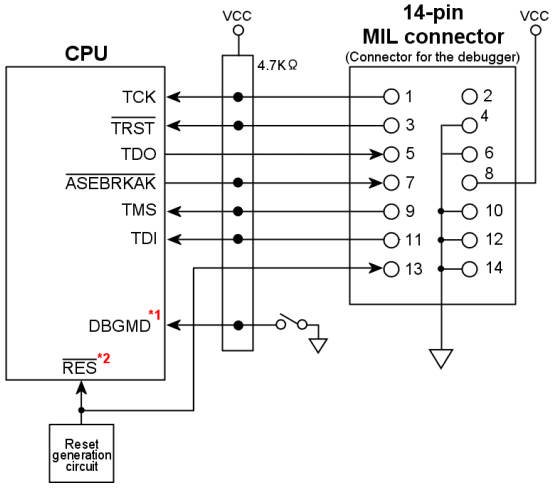
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7144F QFP-112	CPU Pin No. SH7145F LQFP-144	Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7144F QFP-112	CPU Pin No. SH7145F LQFP-144
1	TCK	Input	89	143	2	N.C.			
3	$\overline{\text{TRST}}$	Input	86	139	4	GND			
5	TDO	Output	88	142	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	27	35	8	VCC *2	Output		
9	TMS	Input	85	138	10	GND			
11	TDI	Input	87	140	12	GND			
13	$\overline{\text{RES}}$	Output	84	108	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

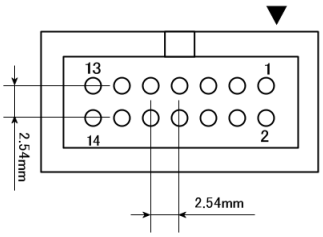
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: To debug, DBGMD pin needs to be brought to High state.
Shown in the target connection reference diagram is the circuit that brings DBGMD pin to High state when you turn OFF the switch.
*2: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

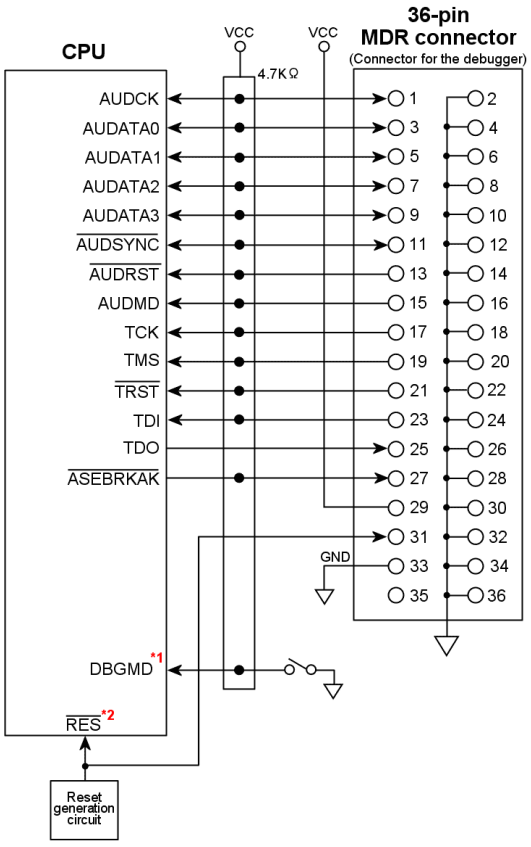
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			SH7144F QFP-112	SH7145F*2 LQFP-144				SH7144F QFP-112	SH7145F*2 LQFP-144
1	AUDCK	Input/Output	53	65/109	2	GND			
3	AUDATA0	Input/Output	60	72/116	4	GND			
5	AUDATA1	Input/Output	59	70/115	6	GND			
7	AUDATA2	Input/Output	58	69/114	8	GND			
9	AUDATA3	Input/Output	57	68/113	10	GND			
11	$\overline{\text{AUDSYNC}}$	Input/Output	52	64/100	12	GND			
13	$\overline{\text{AUDRST}}$	Input	56	67/111	14	GND			
15	AUDMD	Input	54	66/110	16	GND			
17	TCK	Input	89	143	18	GND			
19	TMS	Input	85	138	20	GND			
21	$\overline{\text{TRST}}$	Input	86	139	22	GND			
23	TDI	Input	87	140	24	GND			
25	TDO	Output	88	142	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	27	35	28	GND			
29	VCC*3	Output			30	GND			
31	$\overline{\text{RES}}$	Output	84	108	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For SH7145F, 2 routings of AUD ports are available. Choose either of them.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

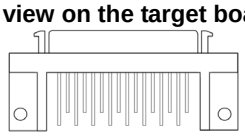
Target connection reference diagram



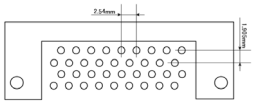
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

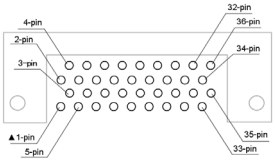
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: To debug, DBGMD pin needs to be brought to High state.
Shown in the target connection reference diagram is the circuit that brings DBGMD pin to High state when you turn OFF the switch.
*2: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7144F/SH7145F)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7146F

Applicable product	PALMiCE3-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

NB : When you use PALMiCE3-SH AUD360 model and if you are using CPU with voltage over 4.0V, please contact us.

MIL connector

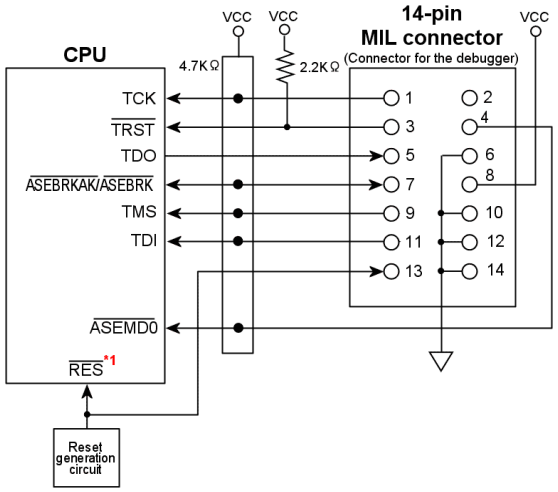
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-80	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-80
1	TCK	Input	7	2	N.C.		
3	$\overline{\text{TRST}}$	Input	1	4	GND($\overline{\text{ASEMD0}}$)*2	(Input)	(56)
5	TDO	Output	3	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/ Output	8	8	VCC *3	Output	
9	TMS	Input	2	10	GND		
11	TDI	Input	5	12	GND		
13	$\overline{\text{RES}}$	Output	52	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

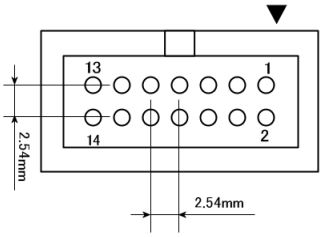
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7146F)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Aug. 2, 2010	Added the note on the use of PALMiCE3-SH AUD360 model.

SH7149F

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

NB : When you use PALMiCE3-SH AUD360 model and if you are using CPU with voltage over 4.0V, please contact us.

MIL connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			QFP-100	LQFP-100				QFP-100	LQFP-100
1	TCK	Input	6	3	2	N.C.			
3	$\overline{\text{TRST}}$	Input	2	99	4	GND($\overline{\text{ASEMD0}}$)*2	(Input)	(71)	(68)
5	TDO	Output	4	1	6	GND			
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/ Output	7	4	8	VCC *3	Output		
9	TMS	Input	3	100	10	GND			
11	TDI	Input	5	2	12	GND			
13	$\overline{\text{RES}}$	Output	67	64	14	GND			

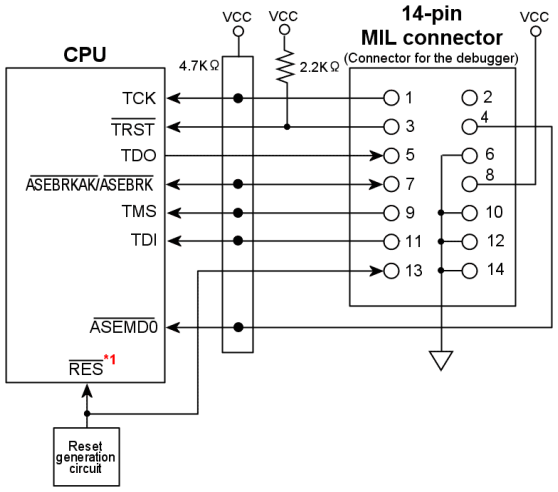
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

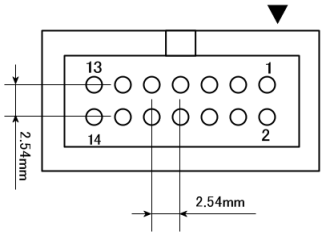
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP-100	CPU Pin No. LQFP-100	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP-100	CPU Pin No. LQFP-100
1	AUDCK	Output	31	28	2	GND			
3	AUDATA0	Output	37	34	4	GND			
5	AUDATA1	Output	36	33	6	GND			
7	AUDATA2	Output	35	32	8	GND			
9	AUDATA3	Output	34	31	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	30	27	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	6	3	18	GND			
19	TMS	Input	3	100	20	GND			
21	$\overline{\text{TRST}}$	Input	2	99	22	GND($\overline{\text{ASEMD0}}$)*2	(Input)	(71)	(68)
23	TDI	Input	5	2	24	GND			
25	TDO	Output	4	1	26	GND			
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	7	4	28	GND			
29	VCC*3	Output			30	GND			
31	$\overline{\text{RES}}$	Output	67	64	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

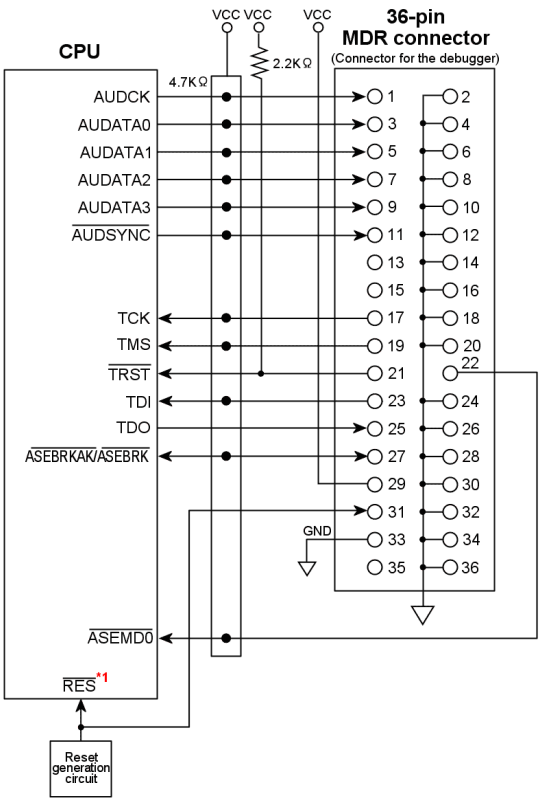
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

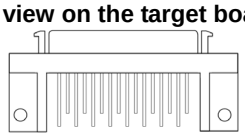
Target connection reference diagram



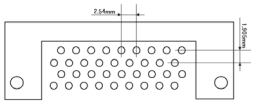
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

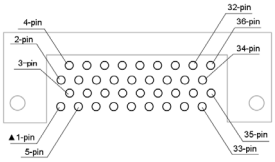
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7149F)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Aug. 2, 2010	Added the note on the use of PALMiCE3-SH AUD360 model.

SH7606

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

MIL connector

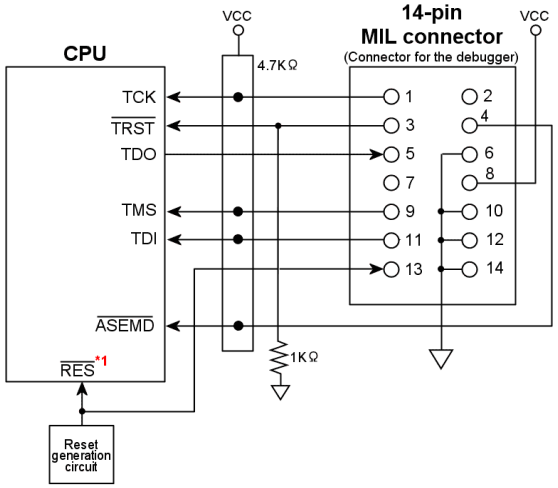
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. BP-176V	Pin No.	Signal	Input/ Output*1	CPU Pin No. BP-176V
1	TCK	Input	N10	2	N.C.		
3	$\overline{\text{TRST}}$	Input	M11	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(N12)
5	TDO	Output	N11	6	GND		
7	N.C.			8	VCC *3	Output	
9	TMS	Input	P11	10	GND		
11	TDI	Input	R11	12	GND		
13	$\overline{\text{RES}}$	Output	R12	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

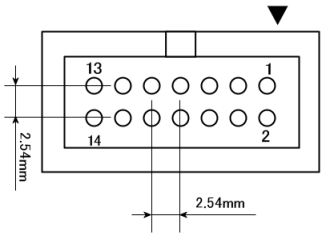
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7606)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7618/SH7618A

Applicable products*1	PALMiCE3-SH / PALMiCE2-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

***1: SH7618A is not supported by PALMiCE2-SH.**

MIL connector

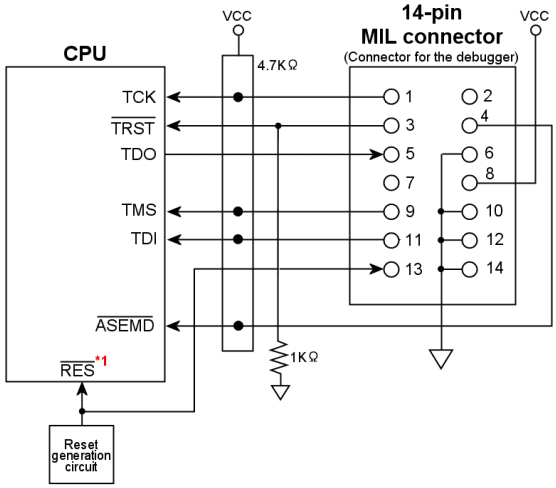
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0176GA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0176GA-A
1	TCK	Input	N10	2	N.C.		
3	$\overline{\text{TRST}}$	Input	M11	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(N12)
5	TDO	Output	N11	6	GND		
7	N.C.			8	VCC *3	Output	
9	TMS	Input	P11	10	GND		
11	TDI	Input	R11	12	GND		
13	$\overline{\text{RES}}$	Output	R12	14	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

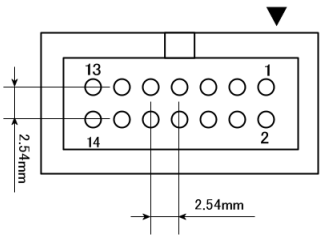
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7618/SH7618A)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following its release. Also, added CPU SH7618A.

SH7619

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

MIL connector

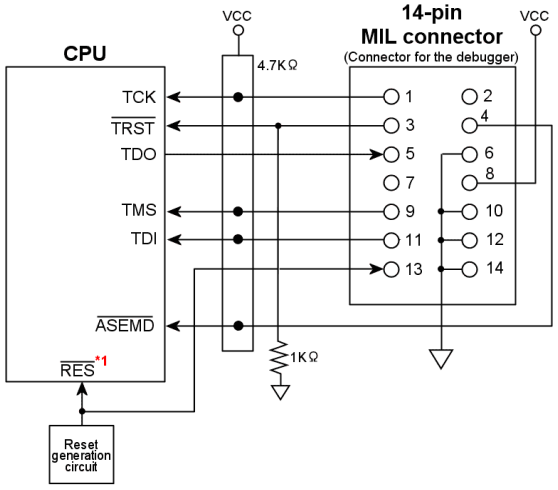
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0176GA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0176GA-A
1	TCK	Input	P12	2	N.C.		
3	$\overline{\text{TRST}}$	Input	M14	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(L13)
5	TDO	Output	N12	6	GND		
7	N.C.			8	VCC *3	Output	
9	TMS	Input	M13	10	GND		
11	TDI	Input	M12	12	GND		
13	$\overline{\text{RES}}$	Output	M15	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

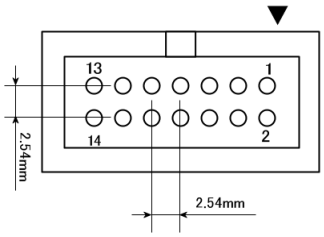
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7619)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH2-DSP

SH7615
SH7616

SH7615

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

MIL connector

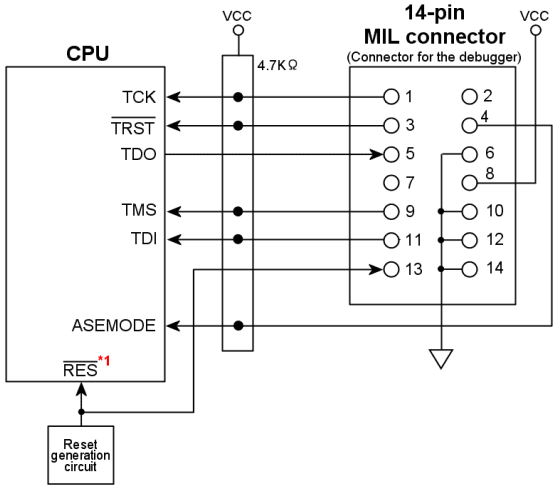
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208 KA-A	CPU Pin No. PLBG0240 JA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208 KA-A	CPU Pin No. PLBG0240 JA-A
1	TCK	Input	30	L1	2	N.C.			
3	$\overline{\text{TRST}}$	Input	32	M3	4	GND (ASEMODE)*2	(Input)	(6)	(E2)
5	TDO	Output	28	L4	6	GND			
7	N.C.				8	VCC *3	Output		
9	TMS	Input	31	M4	10	GND			
11	TDI	Input	29	L2	12	GND			
13	$\overline{\text{RES}}$	Output	8	D3	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, ASEMODE pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings ASEMODE pin to Low state when you connect ASEMODE signal to the connector for debugger.
If you do not connect ASEMODE signal to Pin No. 4 of the connector for debugger, the circuit that sets ASEMODE pin by switch circuit will do. However, in such case, do not connect ASEMODE pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

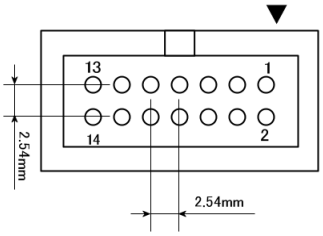
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7615)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7616

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

MIL connector

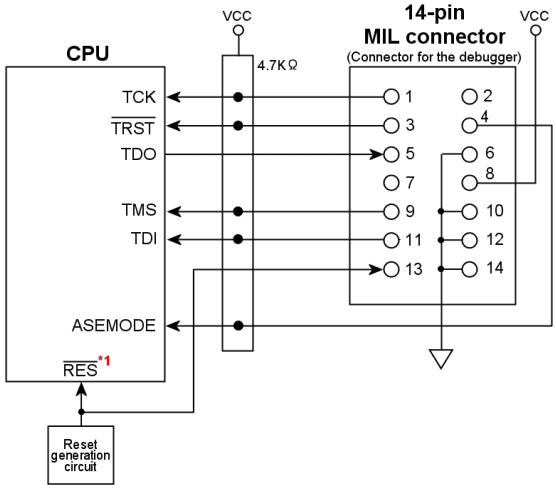
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KA-A
1	TCK	Input	30	2	N.C.		
3	$\overline{\text{TRST}}$	Input	32	4	GND(ASEMODE)*2	(Input)	(6)
5	TDO	Output	28	6	GND		
7	N.C.			8	VCC *3	Output	
9	TMS	Input	31	10	GND		
11	TDI	Input	29	12	GND		
13	$\overline{\text{RES}}$	Output	8	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, ASEMODE pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings ASEMODE pin to Low state when you connect ASEMODE signal to the connector for debugger.
If you do not connect ASEMODE signal to Pin No. 4 of the connector for debugger, the circuit that sets ASEMODE pin by switch circuit will do. However, in such case, do not connect ASEMODE pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

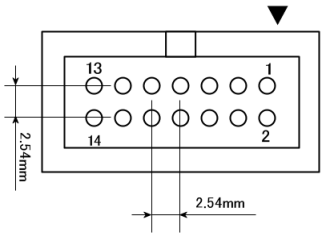
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7616)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH-2A

SH7206
SH7211F
SH7243F/SH7285F/ SH7286F

SH7206

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

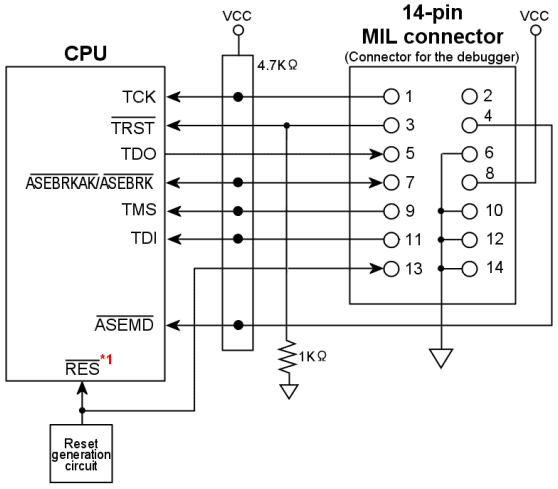
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-176	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-176
1	TCK	Input	110	2	N.C.		
3	$\overline{\text{TRST}}$	Input	111	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(119)
5	TDO	Output	120	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	104	8	VCC *3	Output	
9	TMS	Input	116	10	GND		
11	TDI	Input	112	12	GND		
13	$\overline{\text{RES}}$	Output	37	14	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

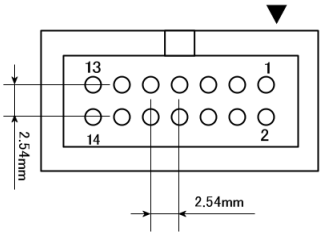
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

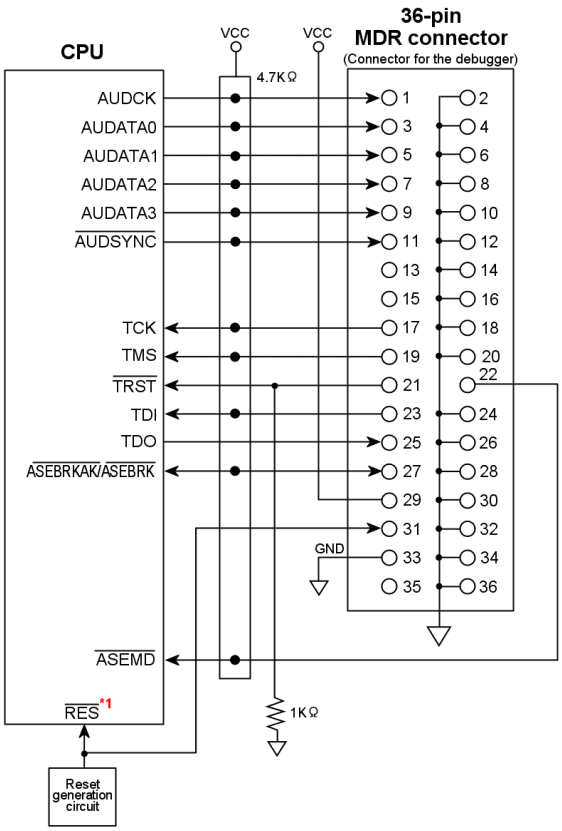
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 LQFP-176	Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 LQFP-176
1	AUDCK	Output	75/134	2	GND		
3	AUDATA0	Output	84/140	4	GND		
5	AUDATA1	Output	82/139	6	GND		
7	AUDATA2	Output	86/138	8	GND		
9	AUDATA3	Output	80/137	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	132/167	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	110	18	GND		
19	TMS	Input	116	20	GND		
21	$\overline{\text{TRST}}$	Input	111	22	GND($\overline{\text{ASEMD}}$)*3	(Input)	(119)
23	TDI	Input	112	24	GND		
25	TDO	Output	120	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	104	28	GND		
29	VCC *4	Output		30	GND		
31	$\overline{\text{RES}}$	Output	37	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: 2 routings of AUD ports are available. Choose either of them.
*3: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*4: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

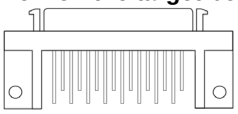
Target connection reference diagram



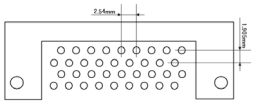
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

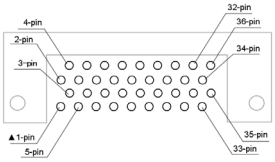
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

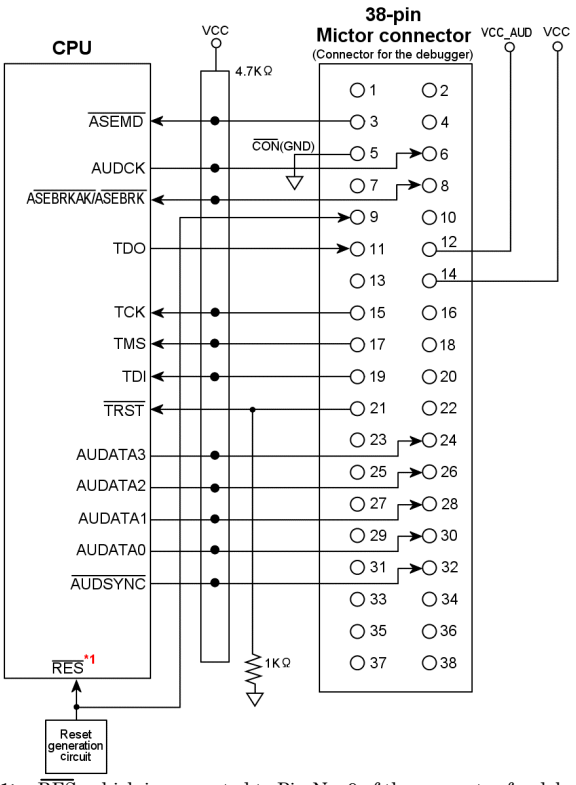
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 LQFP-176	Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 LQFP-176
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *3	(Input)	(119)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *6	(Output)		6	AUDCK	Output	75/134
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	104
9	$\overline{\text{RES}}$	Output	37	10	N.C.		
11	TDO	Output	120	12	VCC_AUD *4	Output	
13	N.C.			14	VCC *5	Output	
15	TCK	Input	110	16	N.C.		
17	TMS	Input	116	18	N.C.		
19	TDI	Input	112	20	N.C.		
21	$\overline{\text{TRST}}$	Input	111	22	N.C.		
23	N.C.			24	AUDATA3	Output	80/137
25	N.C.			26	AUDATA2	Output	86/138
27	N.C.			28	AUDATA1	Output	82/139
29	N.C.			30	AUDATA0	Output	84/140
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output	132/167
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: 2 routings of AUD ports are available. Choose either of them.
*3: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger. If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*4: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*5: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*6: By detection of GND on the target system side, whether the target system is connected or not is determined.

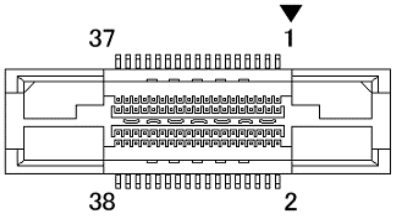
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7206)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.
Third Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7211F

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

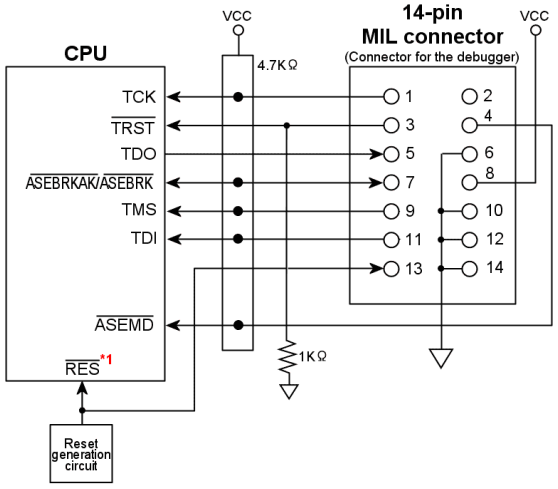
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-144	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-144
1	TCK	Input	16	2	N.C.		
3	$\overline{\text{TRST}}$	Input	18	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(29)
5	TDO	Output	15	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	30	8	VCC *3	Output	
9	TMS	Input	17	10	GND		
11	TDI	Input	12	12	GND		
13	$\overline{\text{RES}}$	Output	22	14	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

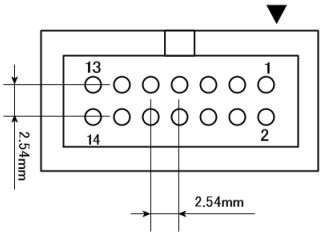
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-144	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-144
1	AUDCK	Output	110	2	GND		
3	AUDATA0	Output	116	4	GND		
5	AUDATA1	Output	115	6	GND		
7	AUDATA2	Output	112	8	GND		
9	AUDATA3	Output	111	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	109	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	16	18	GND		
19	TMS	Input	17	20	GND		
21	$\overline{\text{TRST}}$	Input	18	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(29)
23	TDI	Input	12	24	GND		
25	TDO	Output	15	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	30	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	22	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

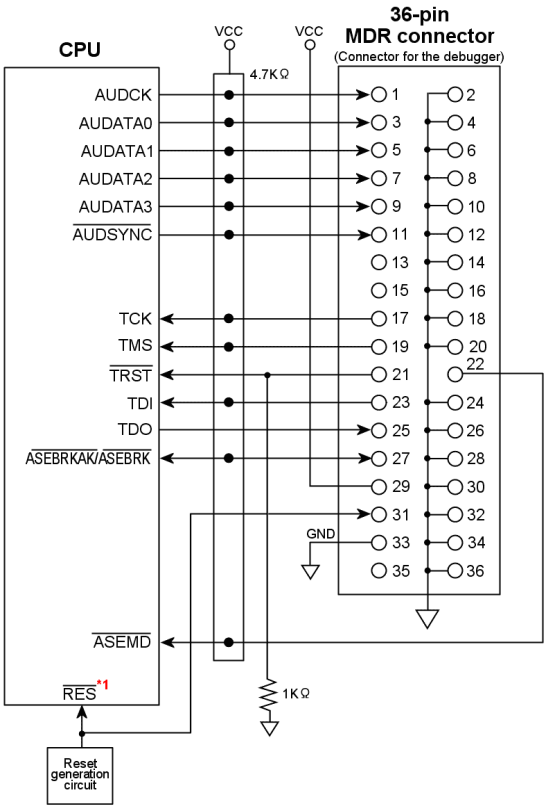
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

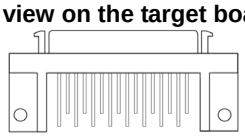
Target connection reference diagram



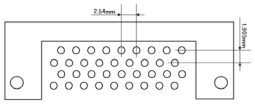
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

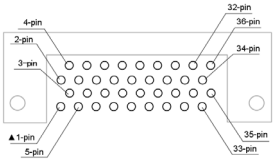
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-144	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP-144
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(29)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output	110
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	30
9	$\overline{\text{RES}}$	Output	22	10	N.C.		
11	TDO	Output	15	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	16	16	N.C.		
17	TMS	Input	17	18	N.C.		
19	TDI	Input	12	20	N.C.		
21	$\overline{\text{TRST}}$	Input	18	22	N.C.		
23	N.C.			24	AUDATA3	Output	111
25	N.C.			26	AUDATA2	Output	112
27	N.C.			28	AUDATA1	Output	115
29	N.C.			30	AUDATA0	Output	116
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output	109
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

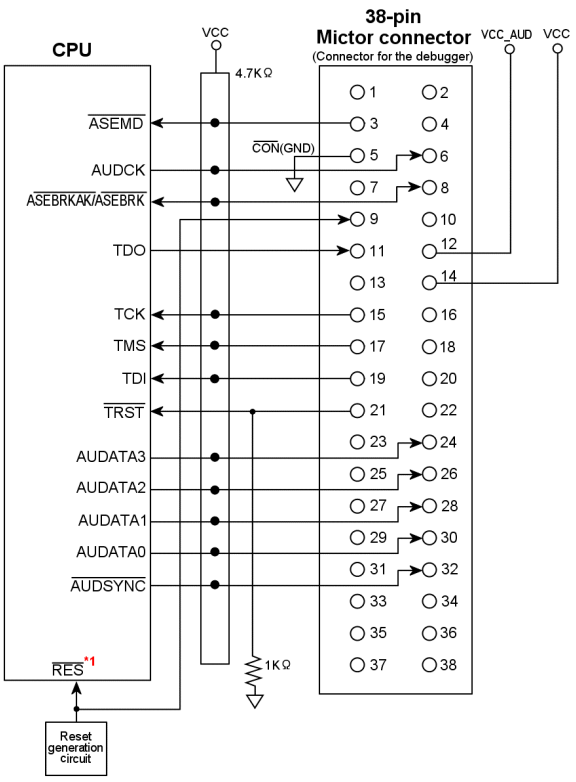
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger. If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.

*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.

*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.

*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

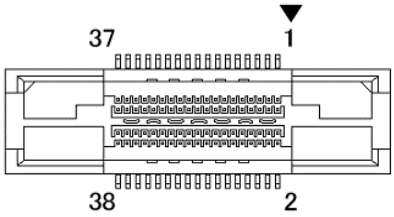
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7211F)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7243F/SH7285F/ SH7286F

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

NB : When you use PALMiCE3-SH AUD360 model and if you are using CPU with voltage over 4.0V, please contact us.

MIL connector

Signals

Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7243F LQFP-100 (FP-100UV)	CPU Pin No. SH7285F LQFP-144 (FP-144LV)	CPU Pin No. SH7286F LQFP-176 (FP-176AV, FP-176EV)	Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7243F LQFP-100 (FP-100UV)	CPU Pin No. SH7285F LQFP-144 (FP-144LV)	CPU Pin No. SH7286F LQFP-176 (FP-176AV, FP-176EV)
1	TCK	Input	8	133	91	2	N.C.				
3	$\overline{\text{TRST}}$	Input	10	135	93	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(78)	(115)	(135)
5	TDO	Output	7	132	90	6	GND				
7	$\overline{\text{ASEBRKAK}}$/ $\overline{\text{ASEBRK}}$	Input/ Output	77	114	134	8	VCC *3	Output			
9	TMS	Input	9	134	92	10	GND				
11	TDI	Input	6	131	89	12	GND				
13	$\overline{\text{RES}}$	Output	76	113	133	14	GND				

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

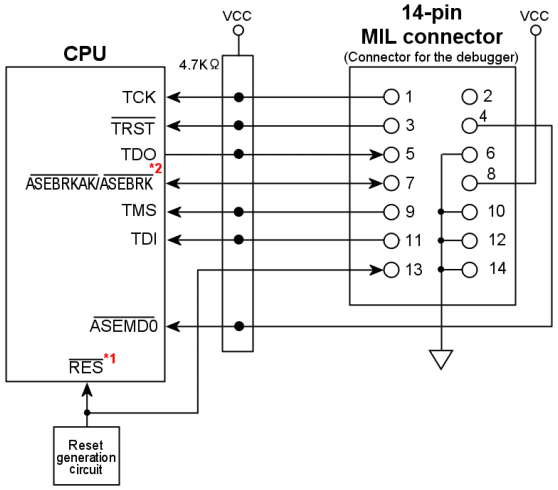
*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.

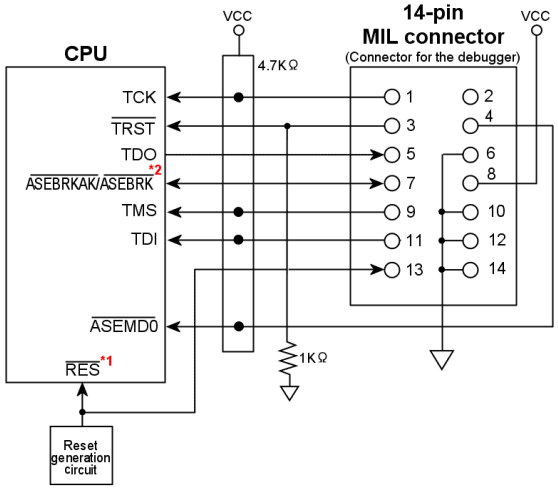
*3: For VCC, connect I/O power of CPU.

Target connection reference diagram

SH7243F/SH7285F



SH7286F



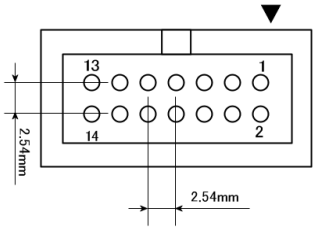
*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

*2: $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ (Output/Input signals) are multiplexed with FWE (Input signal) in a pin. To allow the operation of the user target alone when you use the ICE, in making signal arrangement, do not connect the pin to VCC nor GND directly, but connect it to a pull-up resistor with ohmic value of 4.7K or a pull-down resistor with ohmic value of 100k.

MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

MDR connector

Signals

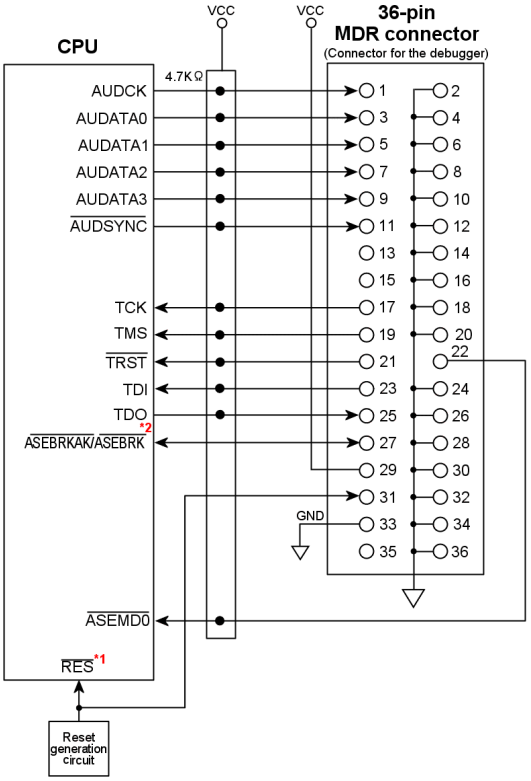
Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7243F LQFP-100 (FP-100UV)	CPU Pin No. SH7285F LQFP-144 (FP-144LV)	CPU Pin No. SH7286F LQFP-176 (FP-176AV, FP-176EV)	Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7243F LQFP-100 (FP-100UV)	CPU Pin No. SH7285F LQFP-144 (FP-144LV)	CPU Pin No. SH7286F LQFP-176 (FP-176AV, FP-176EV)
1	AUDCK	Output	41	64	65	2	GND				
3	AUDATA0	Output	35	57	57	4	GND				
5	AUDATA1	Output	36	58	58	6	GND				
7	AUDATA2	Output	37	59	59	8	GND				
9	AUDATA3	Output	38	60	60	10	GND				
11	$\overline{\text{AUDSYNC}}$	Output	34	63	63	12	GND				
13	N.C.					14	GND				
15	N.C.					16	GND				
17	TCK	Input	8	133	91	18	GND				
19	TMS	Input	9	134	92	20	GND				
21	$\overline{\text{TRST}}$	Input	10	135	93	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(78)	(115)	(135)
23	TDI	Input	6	131	89	24	GND				
25	TDO	Output	7	132	90	26	GND				
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/ Output	77	114	134	28	GND				
29	VCC *3	Output				30	GND				
31	$\overline{\text{RES}}$	Output	76	113	133	32	GND				
33	GND					34	GND				
35	N.C.					36	GND				

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

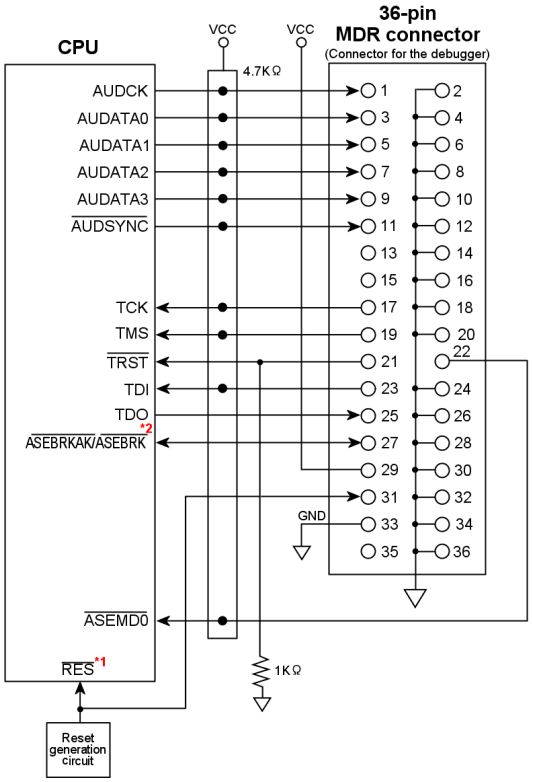
*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU.

Target connection reference diagram

SH7243F/SH7285F



SH7286F

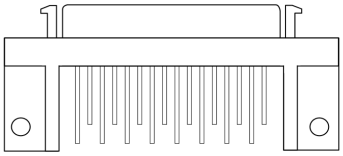


*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.
*2: $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ (Output/Input signals) are multiplexed with FWE (Input signal) in a pin. To allow the operation of the user target alone when you use the ICE, in making signal arrangement, do not connect the pin to VCC nor GND directly, but connect it to a pull-up resistor with ohmic value of 4.7K or a pull-down resistor with ohmic value of 100k.

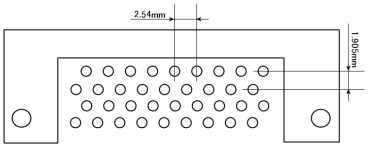
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

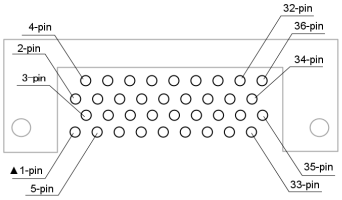
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

Mictor connector

Signals

Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7243F LQFP-100 (FP-100UV)	CPU Pin No. SH7285F LQFP-144 (FP-144LV)	CPU Pin No. SH7286F LQFP-176 (FP-176AV, FP-176EV)	Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7243F LQFP-100 (FP-100UV)	CPU Pin No. SH7285F LQFP-144 (FP-144LV)	CPU Pin No. SH7286F LQFP-176 (FP-176AV, FP-176EV)
1	N.C.					2	N.C.				
3	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(78)	(115)	(135)	4	N.C.				
5	GND ($\overline{\text{CON}}$) *5	(Output)				6	AUDCK	Output	41	64	65
7	N.C.					8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/ Output	77	114	134
9	$\overline{\text{RES}}$	Output	76	113	133	10	N.C.				
11	TDO	Output	7	132	90	12	VCC_AUD*3	Output			
13	N.C.					14	VCC *4	Output			
15	TCK	Input	8	133	91	16	N.C.				
17	TMS	Input	9	134	92	18	N.C.				
19	TDI	Input	6	131	89	20	N.C.				
21	$\overline{\text{TRST}}$	Input	10	135	93	22	N.C.				
23	N.C.					24	AUDATA3	Output	38	60	60
25	N.C.					26	AUDATA2	Output	37	59	59
27	N.C.					28	AUDATA1	Output	36	58	58
29	N.C.					30	AUDATA0	Output	35	57	57
31	N.C.					32	$\overline{\text{AUDSYNC}}$	Output	34	63	63
33	N.C.					34	N.C.				
35	N.C.					36	N.C.				
37	N.C.					38	N.C.				

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.

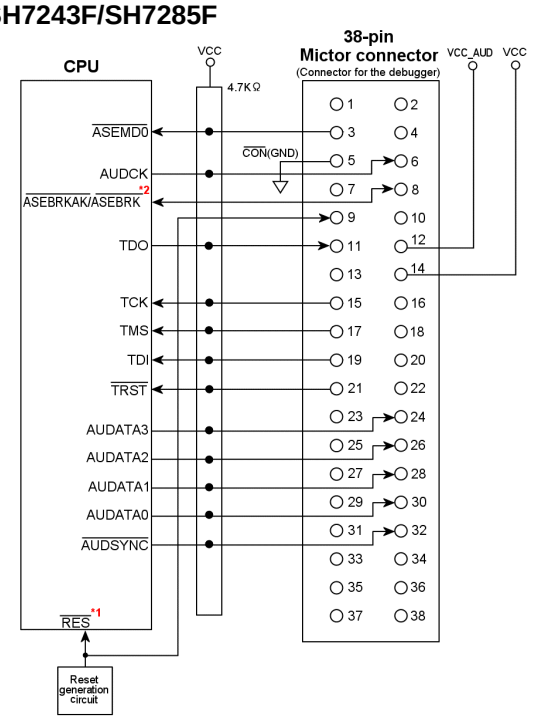
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.

*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.

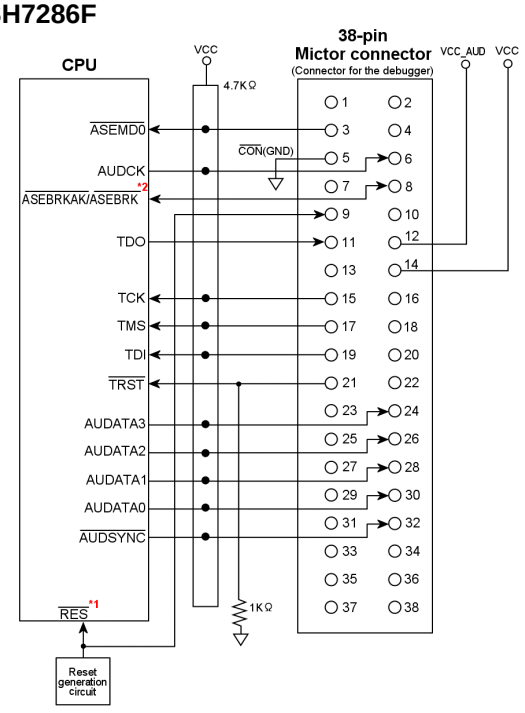
*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

Target connection reference diagram

SH7243F/SH7285F



SH7286F



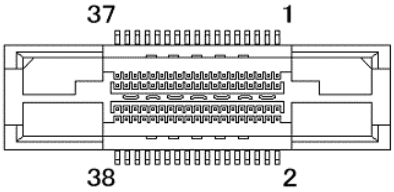
*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

*2: $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ (Output/Input signals) are multiplexed with FWE (Input signal) in a pin. To allow the operation of the user target alone when you use the ICE, in making signal arrangement, do not connect the pin to VCC nor GND directly, but connect it to a pull-up resistor with ohmic value of 4.7K or a pull-down resistor with ohmic value of 100k.

Mictor connector specifications

Recommended connector
- Manufacturer AMP
- Model Mictor connector
  2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

Document change history (SH7243F/SH7285F/ SH7286F)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Sep. 30, 2009	Edited the note on MDR connector.
Third Edition	Jun. 1, 2010	Made provision of support for Mictor connector.
Fourth Edition	Aug. 2. 2010	The note on the use of PALMiCE3-SH AUD360 model given for MDR connector will now apply to all connectors.

SH2A-FPU

SH7201
SH7203
SH7261
SH7262/SH7264
SH7263
SH7670/SH7671/SH7672/SH7673

SH7201

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

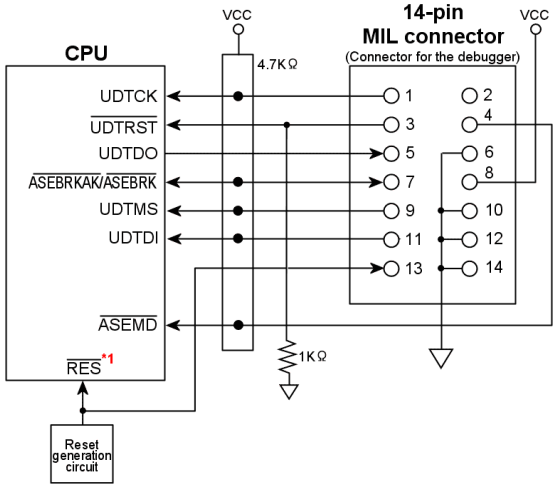
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu
1	UDTCK	Input	131	2	N.C.		
3	$\overline{\text{UDTRST}}$	Input	126	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(133)
5	UDTDO	Output	129	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	132	8	VCC *3	Output	
9	UDTMS	Input	128	10	GND		
11	UDTDI	Input	130	12	GND		
13	$\overline{\text{RES}}$	Output	2	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

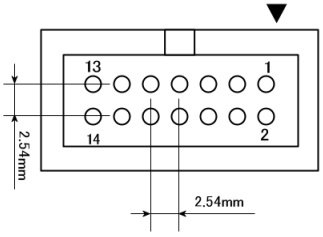
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu
1	AUDCK	Output*4	97	2	GND		
3	AUDATA0	Output*4	99	4	GND		
5	AUDATA1	Output*4	100	6	GND		
7	AUDATA2	Output*4	102	8	GND		
9	AUDATA3	Output*4	104	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output*4	98	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	UDTCK	Input	131	18	GND		
19	UDTMS	Input	128	20	GND		
21	$\overline{\text{UDTRST}}$	Input	126	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(133)
23	UDTDI	Input	130	24	GND		
25	UDTDO	Output	129	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	132	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	2	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

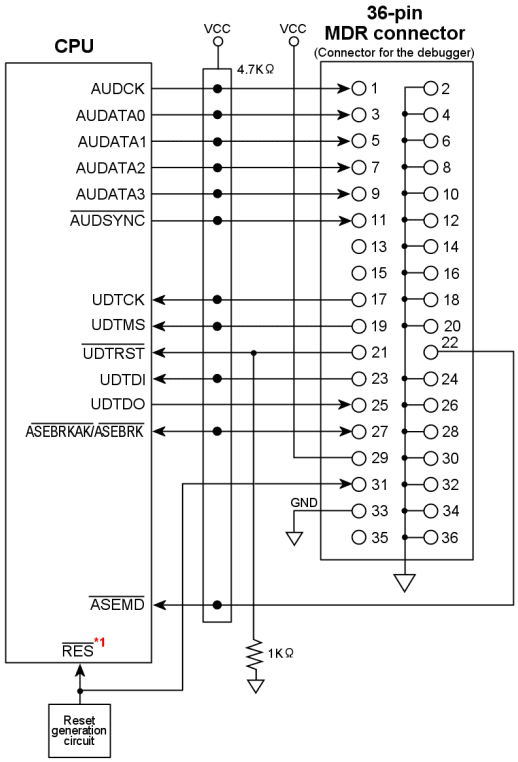
*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

*4: It is used as an output signal as PALMiCE does not support RAM monitor function.

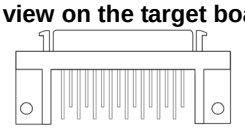
Target connection reference diagram



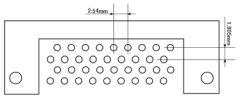
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

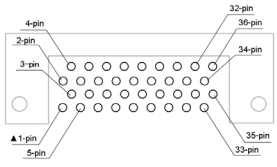
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*: When using the pins multiplexed with AUDMD or $\overline{\text{AUDRST}}$ signal, do not enable AUDMD nor $\overline{\text{AUDRST}}$ signal in Pin Function Controller. When the debugger is used, neither AUDMD nor $\overline{\text{AUDRST}}$ signal is to be used; set the CPU to AUD trace mode. If you enable AUDMD or AUDRST signal, it will inevitably change the setting of AUD.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(133)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output *6	97
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	132
9	$\overline{\text{RES}}$	Output	2	10	N.C.		
11	UDTDO	Output	129	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	UDTCK	Input	131	16	N.C.		
17	UDTMS	Input	128	18	N.C.		
19	UDTDI	Input	130	20	N.C.		
21	$\overline{\text{UDTRST}}$	Input	126	22	N.C.		
23	N.C.			24	AUDATA3	Output *6	104
25	N.C.			26	AUDATA2	Output *6	102
27	N.C.			28	AUDATA1	Output *6	100
29	N.C.			30	AUDATA0	Output *6	99
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output *6	98
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger. If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.

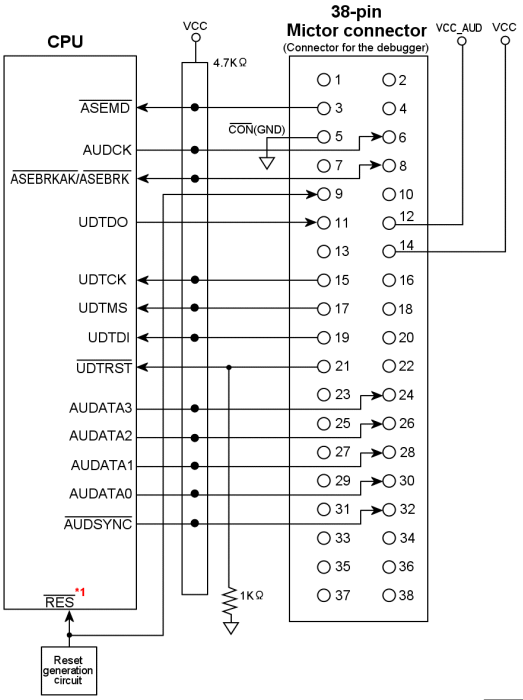
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.

*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.

*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

*6: It is used as an output signal as PALMiCE does not support RAM monitor function.

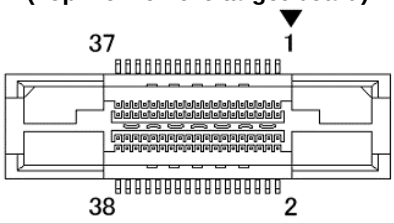
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*: When using the pins multiplexed with AUDMD or $\overline{\text{AUDRST}}$ signal, do not enable AUDMD nor $\overline{\text{AUDRST}}$ signal in Pin Function Controller. When the debugger is used, neither AUDMD nor $\overline{\text{AUDRST}}$ signal is to be used; set the CPU to AUD trace mode. If you enable AUDMD or AUDRST signal, it will inevitably change the setting of AUD.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7201)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	・ Made provision of support for Mictor connector. ・ **MDR connector** Added the note *4 to signal table. Added notes to Target connection reference diagram.

SH7203

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

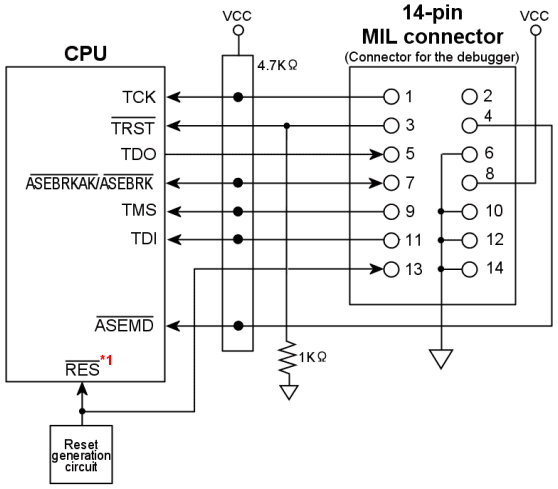
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu
1	TCK	Input	178	2	N.C.		
3	$\overline{\text{TRST}}$	Input	176	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(61)
5	TDO	Output	177	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	175	8	VCC *3	Output	
9	TMS	Input	172	10	GND		
11	TDI	Input	174	12	GND		
13	$\overline{\text{RES}}$	Output	59	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

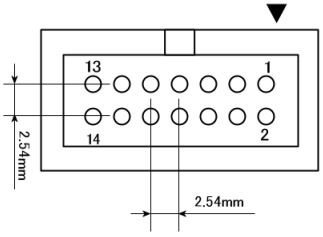
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu
1	AUDCK	Output	122	2	GND		
3	AUDATA0	Output	1	4	GND		
5	AUDATA1	Output	240	6	GND		
7	AUDATA2	Output	142	8	GND		
9	AUDATA3	Output	145	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	17	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	178	18	GND		
19	TMS	Input	172	20	GND		
21	$\overline{\text{TRST}}$	Input	176	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(61)
23	TDI	Input	174	24	GND		
25	TDO	Output	177	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	175	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	59	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

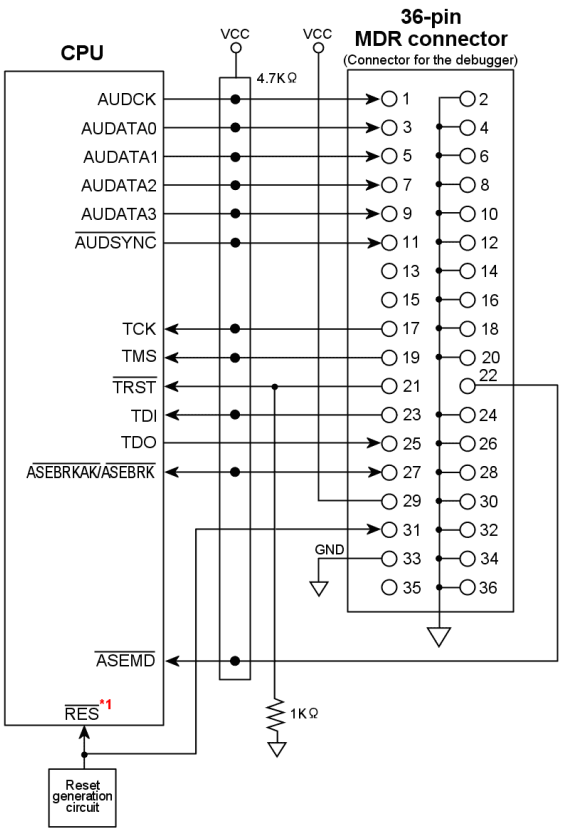
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

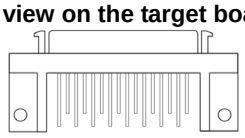
Target connection reference diagram



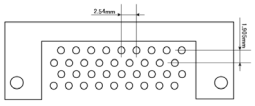
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

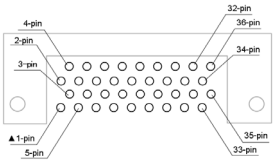
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

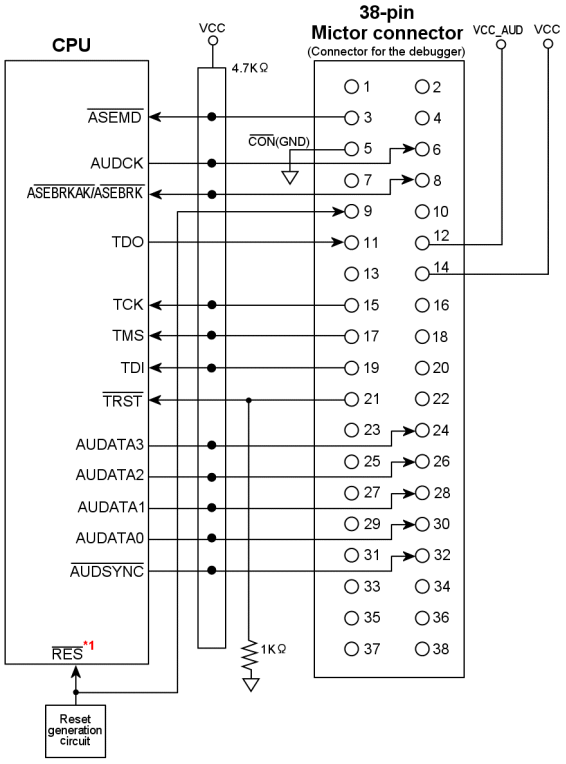
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(61)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output	122
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	175
9	$\overline{\text{RES}}$	Output	59	10	N.C.		
11	TDO	Output	177	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	178	16	N.C.		
17	TMS	Input	172	18	N.C.		
19	TDI	Input	174	20	N.C.		
21	$\overline{\text{TRST}}$	Input	176	22	N.C.		
23	N.C.			24	AUDATA3	Output	145
25	N.C.			26	AUDATA2	Output	142
27	N.C.			28	AUDATA1	Output	240
29	N.C.			30	AUDATA0	Output	1
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output	17
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger. If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

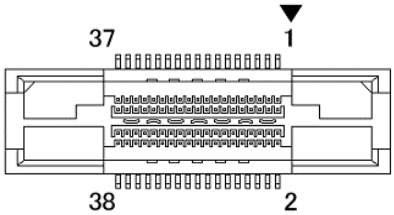
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7203)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7261

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu
1	UDTCK	Input	131	2	N.C.		
3	$\overline{\text{UDTRST}}$	Input	126	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(133)
5	UDTDO	Output	129	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	132	8	VCC *3	Output	
9	UDTMS	Input	128	10	GND		
11	UDTDI	Input	130	12	GND		
13	$\overline{\text{RES}}$	Output	2	14	GND		

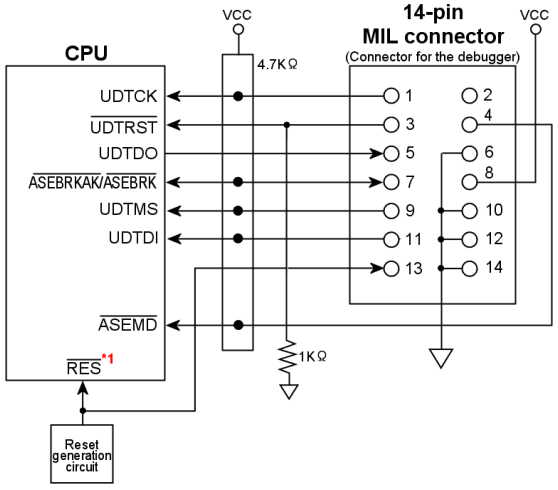
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

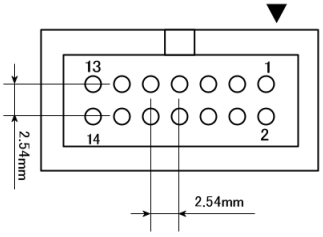
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu
1	AUDCK	Output*4	97	2	GND		
3	AUDATA0	Output*4	99	4	GND		
5	AUDATA1	Output*4	100	6	GND		
7	AUDATA2	Output*4	102	8	GND		
9	AUDATA3	Output*4	104	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output*4	98	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	UDTCK	Input	131	18	GND		
19	UDTMS	Input	128	20	GND		
21	$\overline{\text{UDTRST}}$	Input	126	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(133)
23	UDTDI	Input	130	24	GND		
25	UDTDO	Output	129	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	132	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	2	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

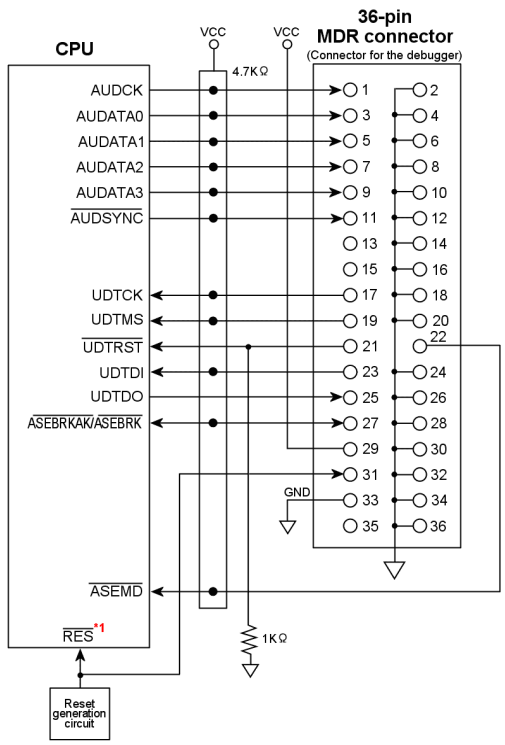
*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

*4: It is used as an output signal as PALMiCE does not support RAM monitor function.

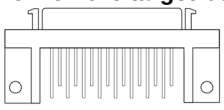
Target connection reference diagram



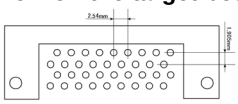
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

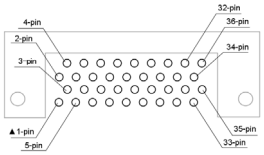
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*: When using the pins multiplexed with AUDMD or $\overline{\text{AUDRST}}$ signal, do not enable AUDMD nor $\overline{\text{AUDRST}}$ signal in Pin Function Controller. When the debugger is used, neither AUDMD nor $\overline{\text{AUDRST}}$ signal is to be used; set the CPU to AUD trace mode. If you enable AUDMD or $\overline{\text{AUDRST}}$ signal, it will inevitably change the setting of AUD.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. LQFP2424 -176Cu
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(133)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output*6	97
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	132
9	$\overline{\text{RES}}$	Output	2	10	N.C.		
11	UDTDO	Output	129	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	UDTCK	Input	131	16	N.C.		
17	UDTMS	Input	128	18	N.C.		
19	UDTDI	Input	130	20	N.C.		
21	$\overline{\text{UDTRST}}$	Input	126	22	N.C.		
23	N.C.			24	AUDATA3	Output *6	104
25	N.C.			26	AUDATA2	Output *6	102
27	N.C.			28	AUDATA1	Output *6	100
29	N.C.			30	AUDATA0	Output *6	99
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output *6	98
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.

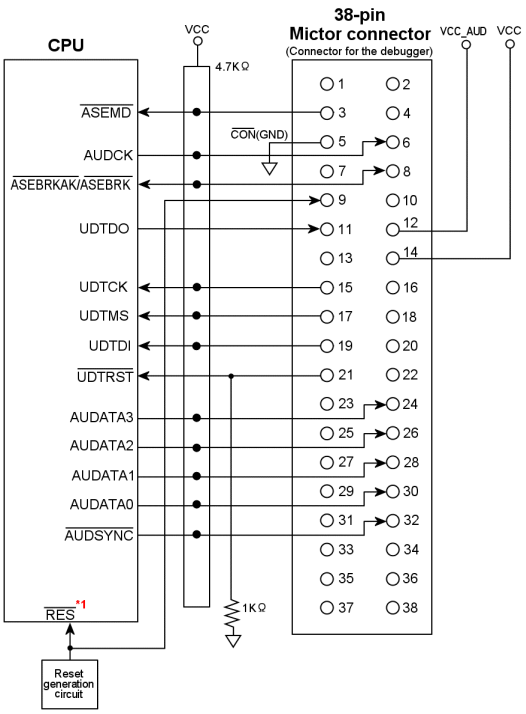
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.

*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.

*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

*6: It is used as an output signal as PALMiCE does not support RAM monitor function.

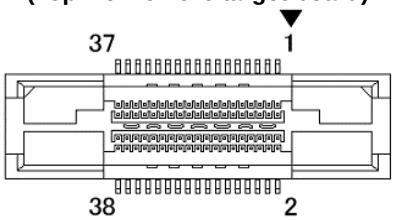
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*: When using the pins multiplexed with AUDMD or $\overline{\text{AUDRST}}$ signal, do not enable AUDMD nor $\overline{\text{AUDRST}}$ signal in Pin Function Controller. When the debugger is used, neither AUDMD nor $\overline{\text{AUDRST}}$ signal is to be used; set the CPU to AUD trace mode. If you enable AUDMD or $\overline{\text{AUDRST}}$ signal, it will inevitably change the setting of AUD.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7261)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	・ Made provision of support for Mictor connector. ・ **MDR connector** Added the note *4 to signal table. Added notes to Target connection reference diagram.

SH7262/SH7264

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

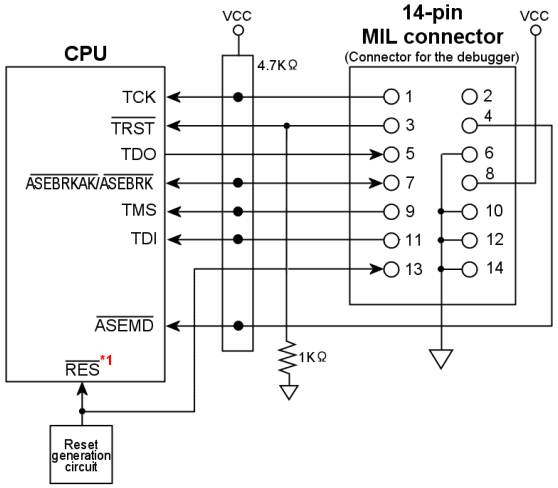
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7262 PLQP0176 KB-A	CPU Pin No. SH7264 PLQP0208 KB-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7262 PLQP0176 KB-A	CPU Pin No. SH7264 PLQP0208 KB-A
1	TCK	Input	94	110	2	N.C.			
3	$\overline{\text{TRST}}$	Input	89	105	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(67)	(79)
5	TDO	Output	91	107	6	GND			
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	90	106	8	VCC *3	Output		
9	TMS	Input	93	109	10	GND			
11	TDI	Input	92	108	12	GND			
13	$\overline{\text{RES}}$	Output	43	51	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

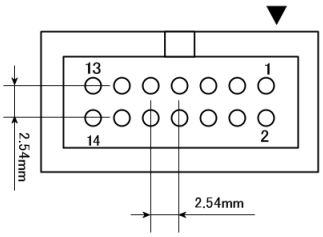
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7262 PLQP0176 KB-A	CPU Pin No. SH7264 PLQP0208 KB-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7262 PLQP0176 KB-A	CPU Pin No. SH7264 PLQP0208 KB-A
1	AUDCK	Output	144	168	2	GND			
3	AUDATA0	Output	140	164	4	GND			
5	AUDATA1	Output	139	163	6	GND			
7	AUDATA2	Output	138	162	8	GND			
9	AUDATA3	Output	137	161	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	142	166	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	94	110	18	GND			
19	TMS	Input	93	109	20	GND			
21	$\overline{\text{TRST}}$	Input	89	105	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(67)	(79)
23	TDI	Input	92	108	24	GND			
25	TDO	Output	91	107	26	GND			
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	90	106	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RES}}$	Output	43	51	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

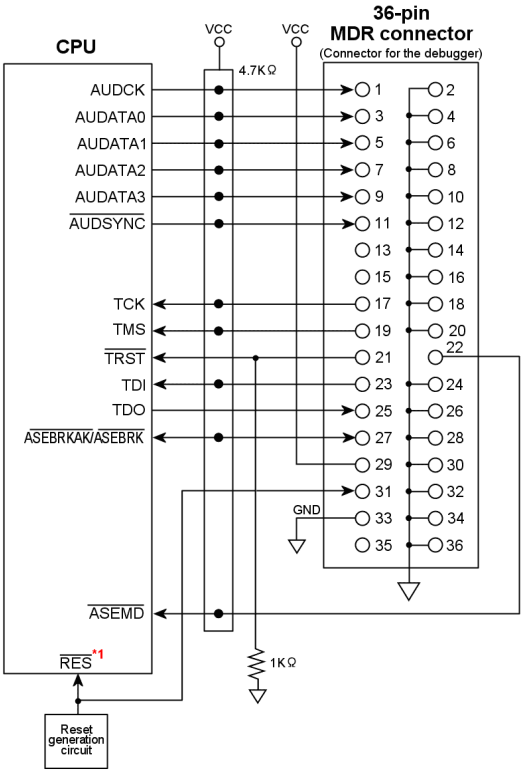
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

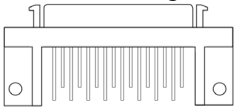
Target connection reference diagram



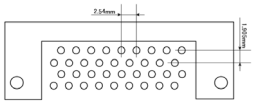
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

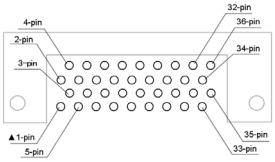
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7262 PLQP0176 KB-A	CPU Pin No. SH7264 PLQP0208 KB-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. SH7262 PLQP0176 KB-A	CPU Pin No. SH7264 PLQP0208 KB-A
1	N.C.				2	N.C.			
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(67)	(79)	4	N.C.			
5	GND($\overline{\text{CON}}$) *5	(Output)			6	AUDCK	Output	144	168
7	N.C.				8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	90	106
9	$\overline{\text{RES}}$	Output	43	51	10	N.C.			
11	TDO	Output	91	107	12	VCC_AUD *3	Output		
13	N.C.				14	VCC *4	Output		
15	TCK	Input	94	110	16	N.C.			
17	TMS	Input	93	109	18	N.C.			
19	TDI	Input	92	108	20	N.C.			
21	$\overline{\text{TRST}}$	Input	89	105	22	N.C.			
23	N.C.				24	AUDATA3	Output	137	161
25	N.C.				26	AUDATA2	Output	138	162
27	N.C.				28	AUDATA1	Output	139	163
29	N.C.				30	AUDATA0	Output	140	164
31	N.C.				32	$\overline{\text{AUDSYNC}}$	Output	142	166
33	N.C.				34	N.C.			
35	N.C.				36	N.C.			
37	N.C.				38	N.C.			

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

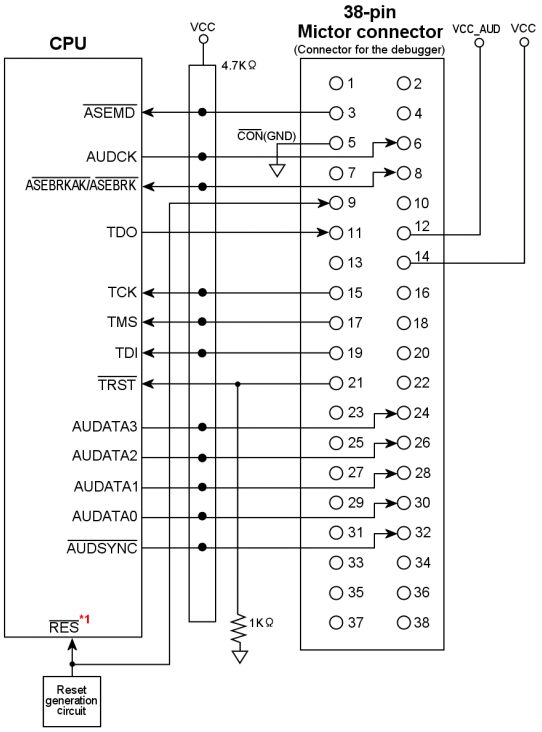
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.

*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.

*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.

*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

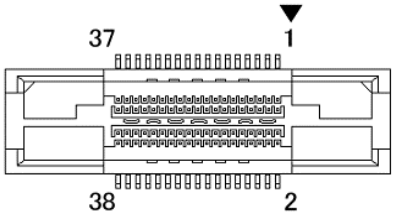
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7262/SH7264)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7263

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

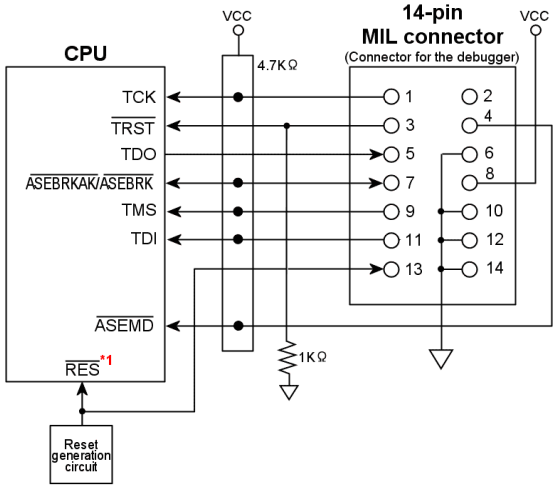
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu
1	TCK	Input	178	2	N.C.		
3	$\overline{\text{TRST}}$	Input	176	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(61)
5	TDO	Output	177	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	175	8	VCC *3	Output	
9	TMS	Input	172	10	GND		
11	TDI	Input	174	12	GND		
13	$\overline{\text{RES}}$	Output	59	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

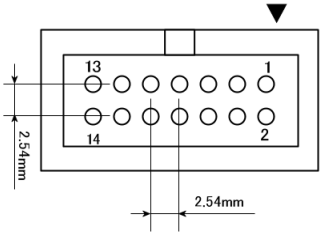
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu
1	AUDCK	Output	122	2	GND		
3	AUDATA0	Output	1	4	GND		
5	AUDATA1	Output	240	6	GND		
7	AUDATA2	Output	142	8	GND		
9	AUDATA3	Output	145	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	17	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	178	18	GND		
19	TMS	Input	172	20	GND		
21	$\overline{\text{TRST}}$	Input	176	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(61)
23	TDI	Input	174	24	GND		
25	TDO	Output	177	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	175	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	59	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

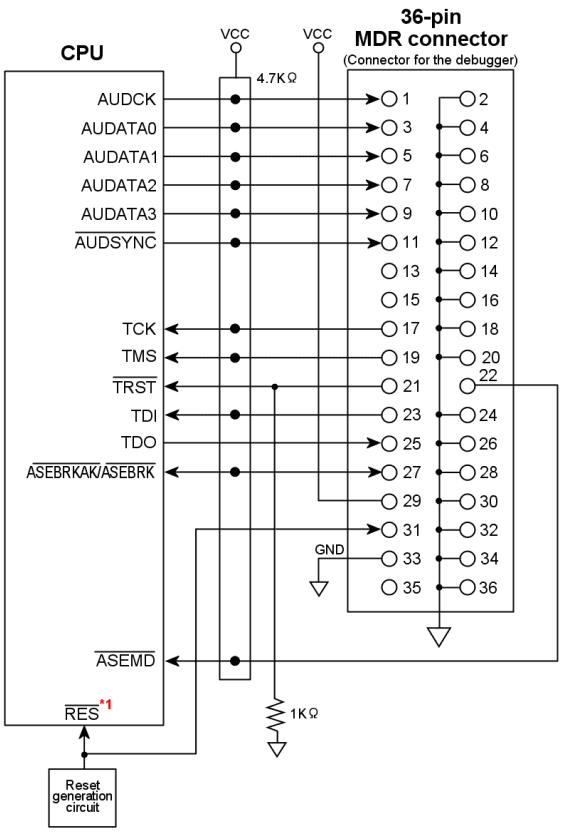
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

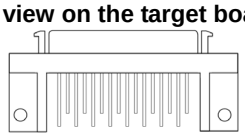
Target connection reference diagram



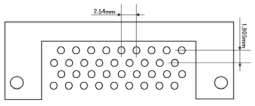
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

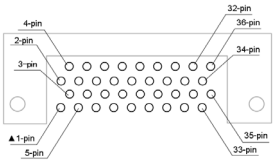
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

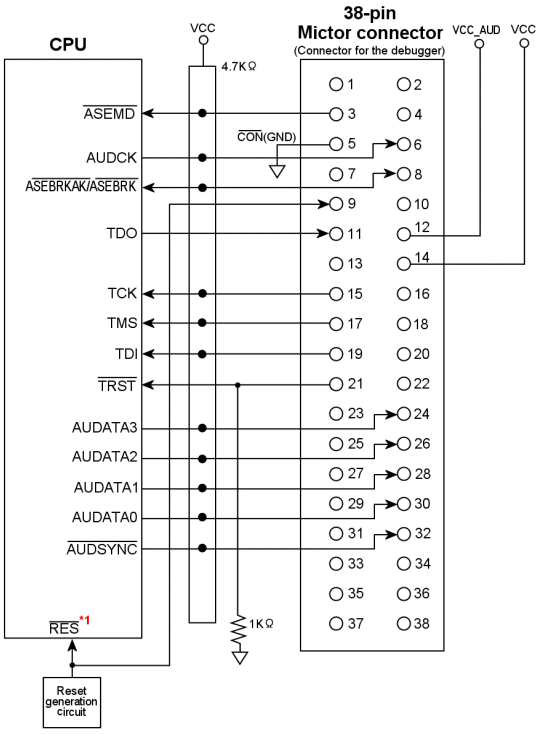
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu	Pin No.	Signal	Input/ Output*1	CPU Pin No. QFP3232 -240Cu
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(61)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output	122
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	175
9	$\overline{\text{RES}}$	Output	59	10	N.C.		
11	TDO	Output	177	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	178	16	N.C.		
17	TMS	Input	172	18	N.C.		
19	TDI	Input	174	20	N.C.		
21	$\overline{\text{TRST}}$	Input	176	22	N.C.		
23	N.C.			24	AUDATA3	Output	145
25	N.C.			26	AUDATA2	Output	142
27	N.C.			28	AUDATA1	Output	240
29	N.C.			30	AUDATA0	Output	1
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output	17
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

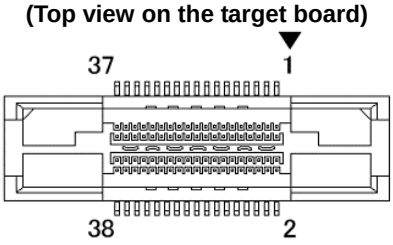
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7263)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7670/SH7671/SH7672/SH7673

Applicable products	PALMiCE3-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

MIL connector

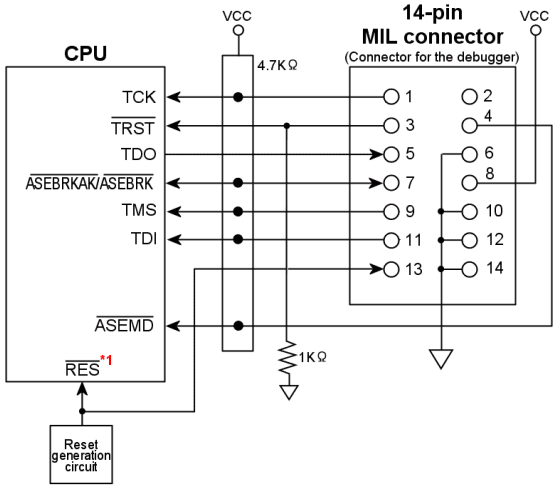
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA256	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA256
1	TCK	Input	V17	2	N.C.		
3	$\overline{\text{TRST}}$	Input	Y18	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(M2)
5	TDO	Output	W19	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	T20	8	VCC *3	Output	
9	TMS	Input	Y19	10	GND		
11	TDI	Input	V18	12	GND		
13	$\overline{\text{RES}}$	Output	W18	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

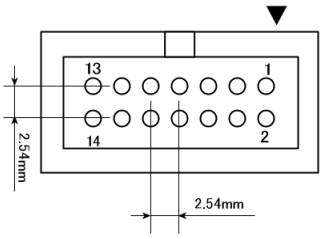
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7670/SH7671/SH7672/SH7673)

First Edition	Jun. 30, 2009	Initial edition

SH2A-DUAL

(Implemented with 2 SH2A-FPUs.)

SH7205
SH7265

SH7205

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

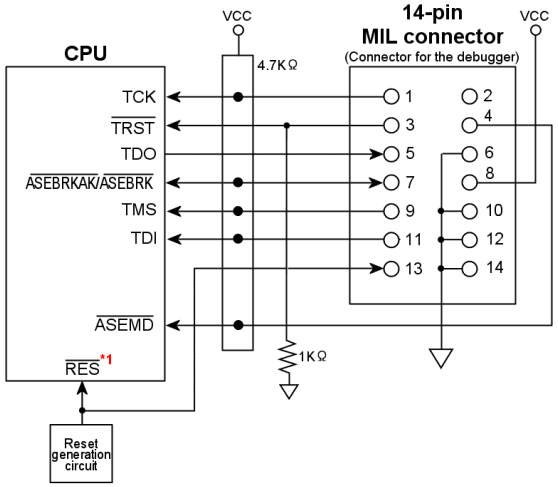
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272
1	TCK	Input	J19	2	N.C.		
3	$\overline{\text{TRST}}$	Input	K20	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(K19)
5	TDO	Output	J20	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	L20	8	VCC *3	Output	
9	TMS	Input	L19	10	GND		
11	TDI	Input	H20	12	GND		
13	$\overline{\text{RES}}$	Output	J17	14	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

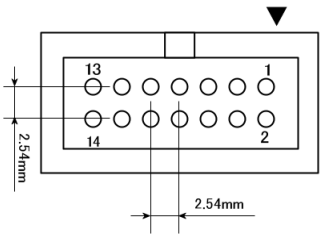
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272
1	AUDCK	Output	W9	2	GND		
3	AUDATA0	Output	U9	4	GND		
5	AUDATA1	Output	Y10	6	GND		
7	AUDATA2	Output	W10	8	GND		
9	AUDATA3	Output	Y11	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	V9	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	J19	18	GND		
19	TMS	Input	L19	20	GND		
21	$\overline{\text{TRST}}$	Input	K20	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(K19)
23	TDI	Input	H20	24	GND		
25	TDO	Output	J20	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	L20	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	J17	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

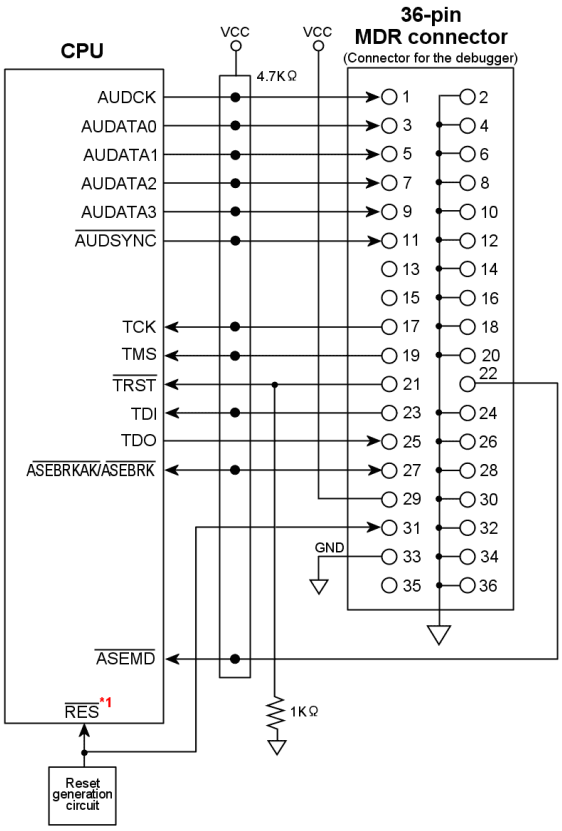
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

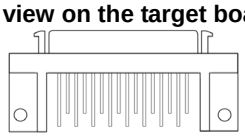
Target connection reference diagram



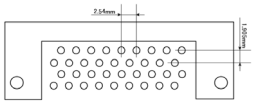
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

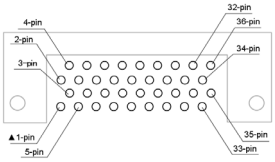
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

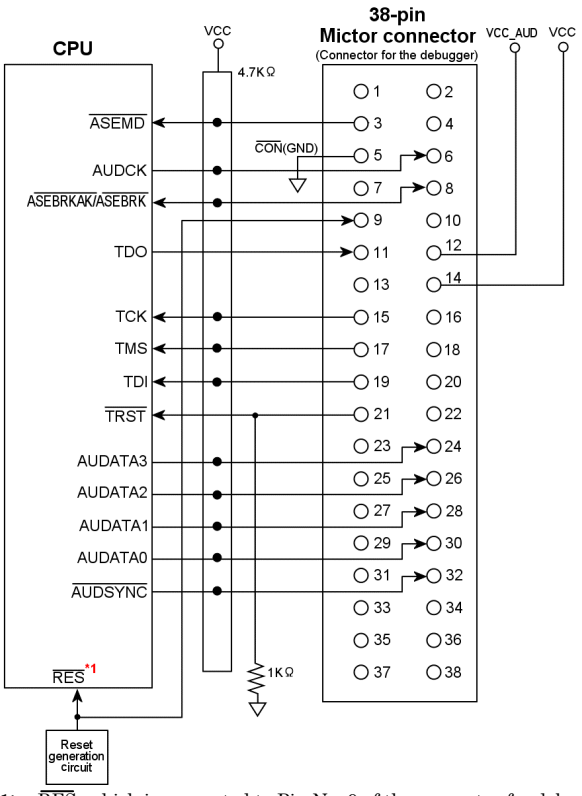
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(K19)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output	W9
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	L20
9	$\overline{\text{RES}}$	Output	J17	10	N.C.		
11	TDO	Output	J20	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	J19	16	N.C.		
17	TMS	Input	L19	18	N.C.		
19	TDI	Input	H20	20	N.C.		
21	$\overline{\text{TRST}}$	Input	K20	22	N.C.		
23	N.C.			24	AUDATA3	Output	Y11
25	N.C.			26	AUDATA2	Output	W10
27	N.C.			28	AUDATA1	Output	Y10
29	N.C.			30	AUDATA0	Output	U9
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output	V9
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger. If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

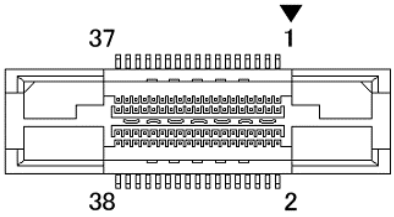
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7205)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7265

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

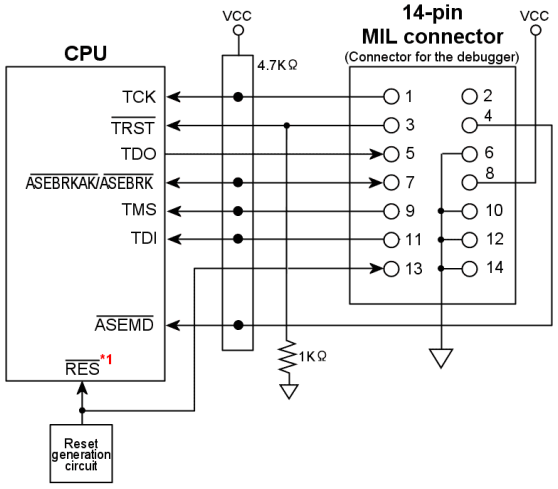
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272
1	TCK	Input	J19	2	N.C.		
3	$\overline{\text{TRST}}$	Input	K20	4	GND($\overline{\text{ASEMD}}$)*2	(Input)	(K19)
5	TDO	Output	J20	6	GND		
7	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	L20	8	VCC *3	Output	
9	TMS	Input	L19	10	GND		
11	TDI	Input	H20	12	GND		
13	$\overline{\text{RES}}$	Output	J17	14	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

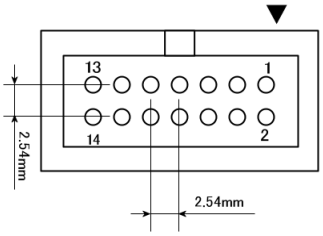
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272
1	AUDCK	Output	W9	2	GND		
3	AUDATA0	Output	U9	4	GND		
5	AUDATA1	Output	Y10	6	GND		
7	AUDATA2	Output	W10	8	GND		
9	AUDATA3	Output	Y11	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	V9	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	J19	18	GND		
19	TMS	Input	L19	20	GND		
21	$\overline{\text{TRST}}$	Input	K20	22	GND($\overline{\text{ASEMD}}$)*2	(Input)	(K19)
23	TDI	Input	H20	24	GND		
25	TDO	Output	J20	26	GND		
27	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	L20	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RES}}$	Output	J17	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

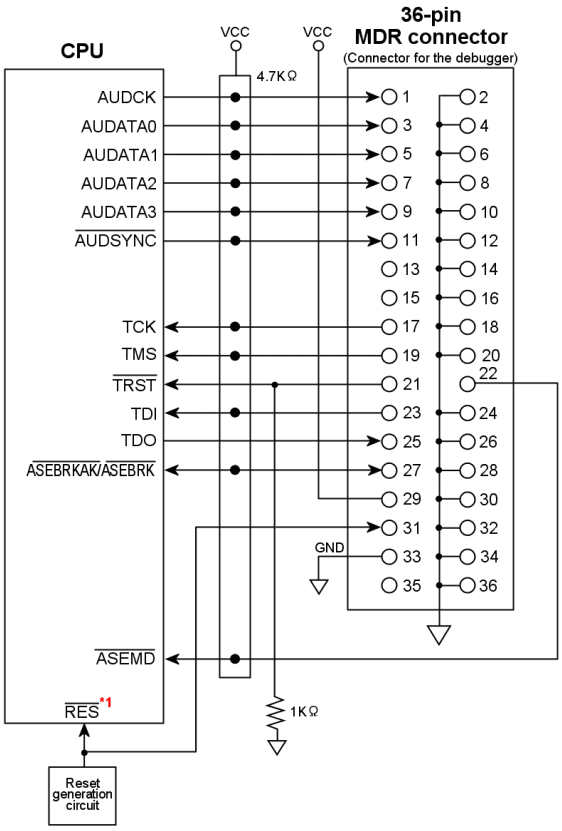
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

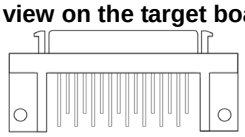
Target connection reference diagram



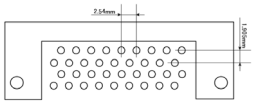
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

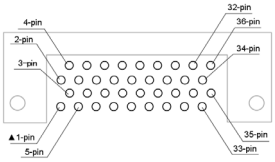
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Mictor connector

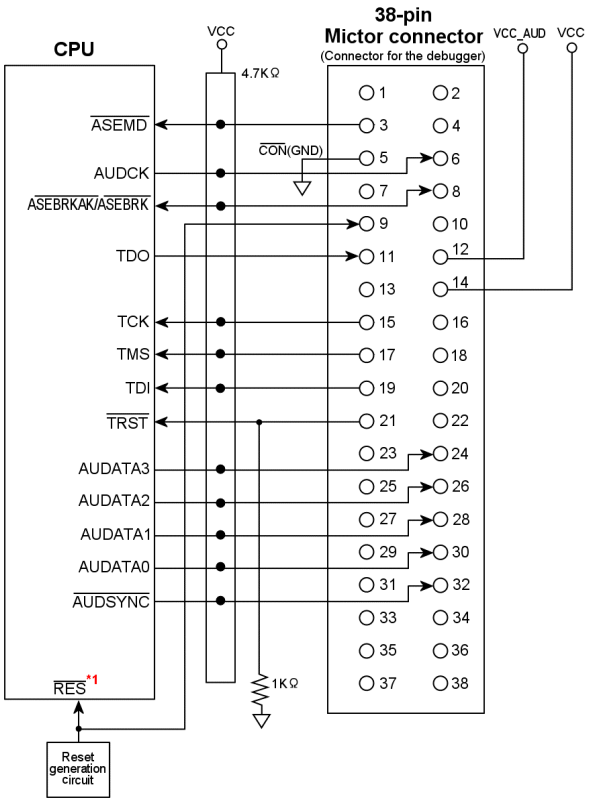
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA272
1	N.C.			2	N.C.		
3	GND ($\overline{\text{ASEMD}}$) *2	(Input)	(K19)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output	W9
7	N.C.			8	$\overline{\text{ASEBRKAK}}$ /$\overline{\text{ASEBRK}}$	Input/Output	L20
9	$\overline{\text{RES}}$	Output	J17	10	N.C.		
11	TDO	Output	J20	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	J19	16	N.C.		
17	TMS	Input	L19	18	N.C.		
19	TDI	Input	H20	20	N.C.		
21	$\overline{\text{TRST}}$	Input	K20	22	N.C.		
23	N.C.			24	AUDATA3	Output	Y11
25	N.C.			26	AUDATA2	Output	W10
27	N.C.			28	AUDATA1	Output	Y10
29	N.C.			30	AUDATA0	Output	U9
31	N.C.			32	$\overline{\text{AUDSYNC}}$	Output	V9
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD}}$ pin to Low state when you connect $\overline{\text{ASEMD}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD}}$ signal to Pin No. 3 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD}}$ pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

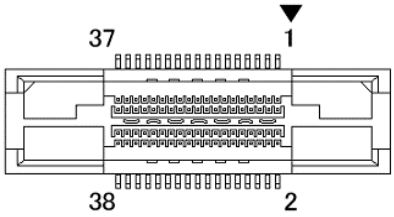
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RES}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RES}}$ pin of CPU.

Document change history (SH7265)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH-3

SH7705
SH7706
SH7709S

SH7705

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

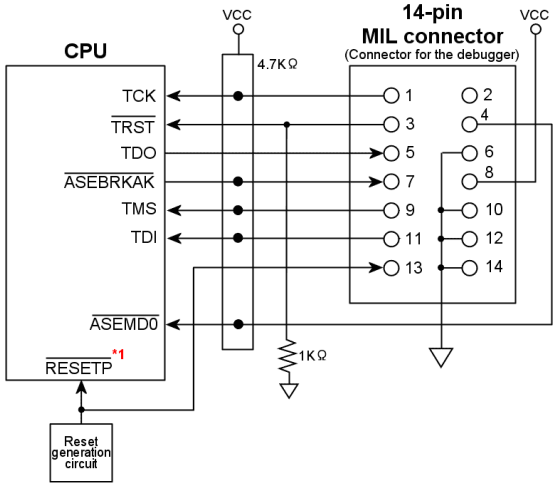
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-208C	CPU Pin No. TBP-208A	Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-208C	CPU Pin No. TBP-208A
1	TCK	Input	140	G14	2	N.C.			
3	$\overline{\text{TRST}}$	Input	142	F16	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(145)	(E17)
5	TDO	Output	143	F15	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	144	F14	8	VCC *3	Output		
9	TMS	Input	141	F17	10	GND			
11	TDI	Input	139	G15	12	GND			
13	$\overline{\text{RESETP}}$	Output	195	C6	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

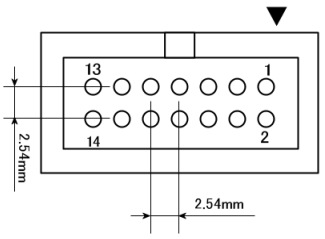
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-208C	TBP-208A				FP-208C	TBP-208A
1	AUDCK	Output	191	C7	2	GND			
3	AUDATA0	Output	118	M15	4	GND			
5	AUDATA1	Output	119	M16	6	GND			
7	AUDATA2	Output	120	M17	8	GND			
9	AUDATA3	Output	121	L14	10	GND			
11	AUDSYNC	Output	117	M14	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	140	G14	18	GND			
19	TMS	Input	141	F17	20	GND			
21	$\overline{\text{TRST}}$	Input	142	F16	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(145)	(E17)
23	TDI	Input	139	G15	24	GND			
25	TDO	Output	143	F15	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	144	F14	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	195	C6	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

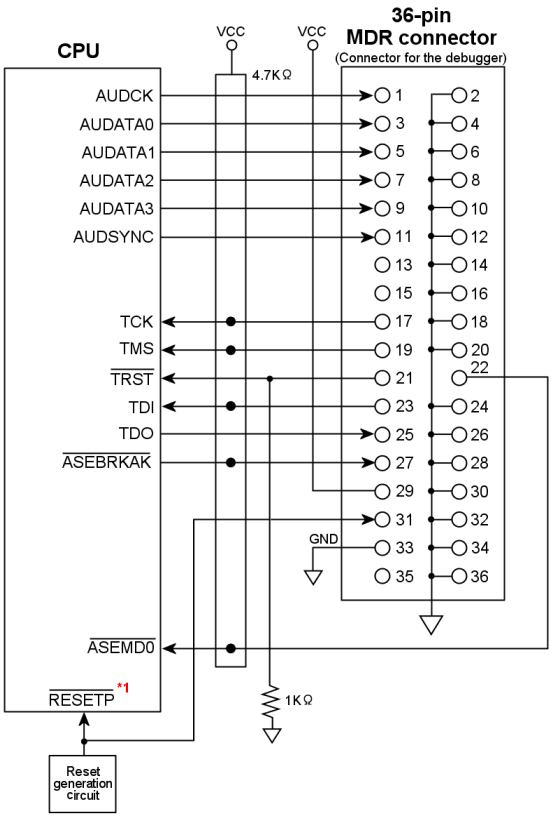
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

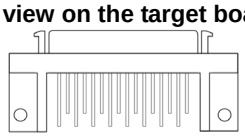
Target connection reference diagram



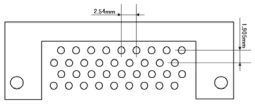
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

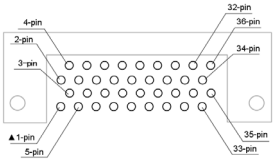
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7705)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	・ **Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.** ・ **Changed the descriptions of AUDSYNC signal regarding the following CPUs.** They had been written in negative logic, however, the descriptions were changed to positive logic so that they conform to the descriptions in the hardware manual published by Renesas Technology Corp..

SH7706

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

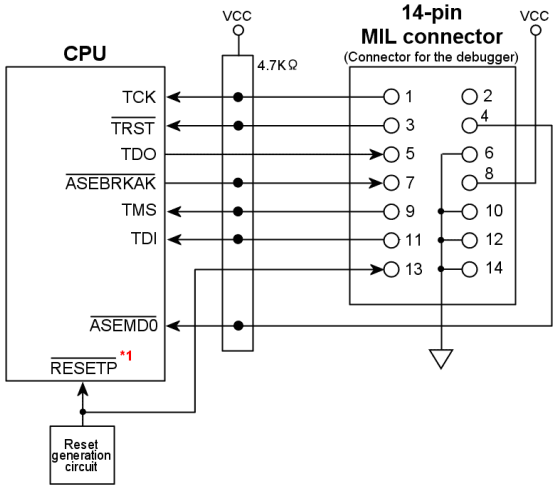
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0176 KD-A	CPU Pin No. TTBG0208 JA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0176 KD-A	CPU Pin No. TTBG0208 JA-A
1	TCK	Input	116	H17	2	N.C.			
3	$\overline{\text{TRST}}$	Input	119	G15	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(122)	(F15)
5	TDO	Output	120	G14	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	121	F16	8	VCC *3	Output		
9	TMS	Input	118	G16	10	GND			
11	TDI	Input	114	J17	12	GND			
13	$\overline{\text{RESETP}}$	Output	165	A6	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

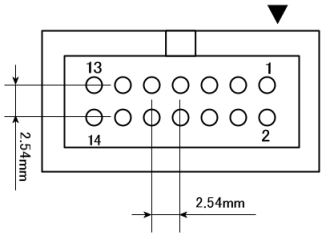
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0176 KD-A	CPU Pin No. TTBG0208 JA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0176 KD-A	CPU Pin No. TTBG0208 JA-A
1	N.C.				2	GND			
3	AUDATA0	Output	109	K15	4	GND			
5	AUDATA1	Output	110	K16	6	GND			
7	AUDATA2	Output	111	K17	8	GND			
9	AUDATA3	Output	112	J14	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	113	J16	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	116	H17	18	GND			
19	TMS	Input	118	G16	20	GND			
21	$\overline{\text{TRST}}$	Input	119	G15	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(122)	(F15)
23	TDI	Input	114	J17	24	GND			
25	TDO	Output	120	G14	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	121	F16	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	165	A6	32	GND			
33	GND				34	GND			
35	AUDCK	Input	159	C9	36	GND			

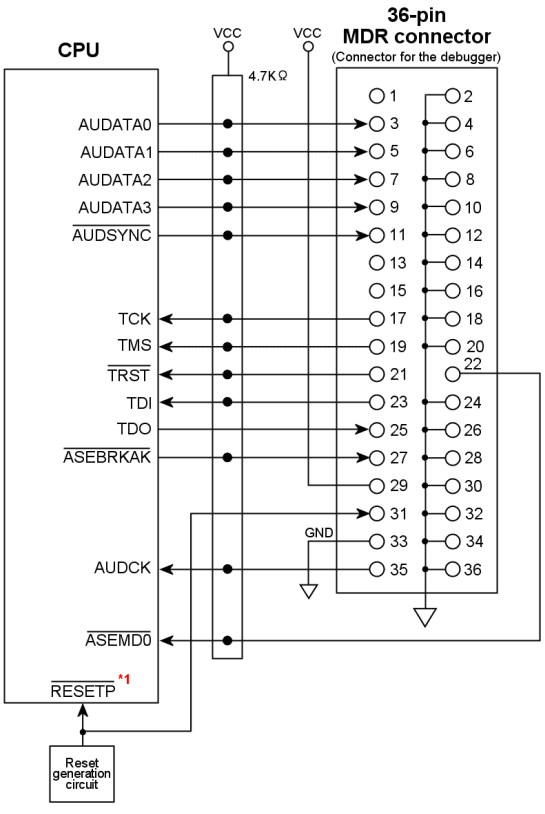
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

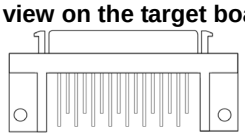
Target connection reference diagram



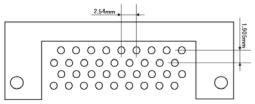
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

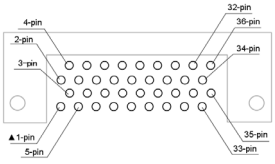
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7706)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7709S

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

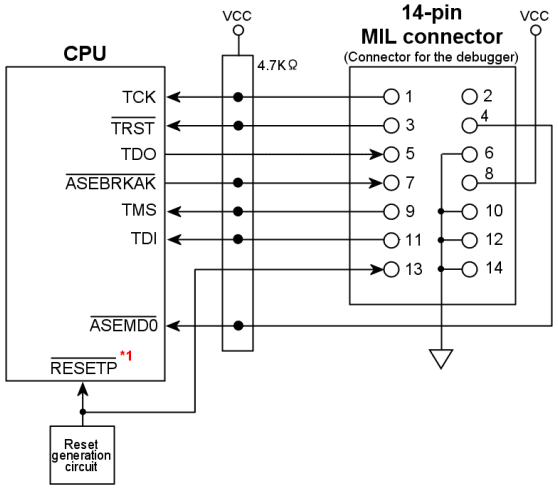
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-208C/E	CPU Pin No. BP-240A	Pin No.	Signal	Input/ Output*1	CPU Pin No. FP-208C/E	CPU Pin No. BP-240A
1	TCK	Input	139	H18	2	N.C.			
3	$\overline{\text{TRST}}$	Input	136	J19	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(127)	(L19)
5	TDO	Output	120	N18	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	128	L18	8	VCC *3	Output		
9	TMS	Input	137	H16	10	GND			
11	TDI	Input	138	H17	12	GND			
13	$\overline{\text{RESETP}}$	Output	193	C7	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

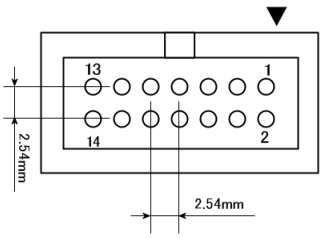
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-208C/E	BP-240A				FP-208C/E	BP-240A
1	N.C.				2	GND			
3	AUDATA0	Output	135	J18	4	GND			
5	AUDATA1	Output	133	K19	6	GND			
7	AUDATA2	Output	131	K18	8	GND			
9	AUDATA3	Output	130	L17	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	94	V14	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	139	H18	18	GND			
19	TMS	Input	137	H16	20	GND			
21	$\overline{\text{TRST}}$	Input	136	J19	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(127)	(L19)
23	TDI	Input	138	H17	24	GND			
25	TDO	Output	120	N18	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	128	L18	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	193	C7	32	GND			
33	GND				34	GND			
35	AUDCK	Input	151	D16	36	GND			

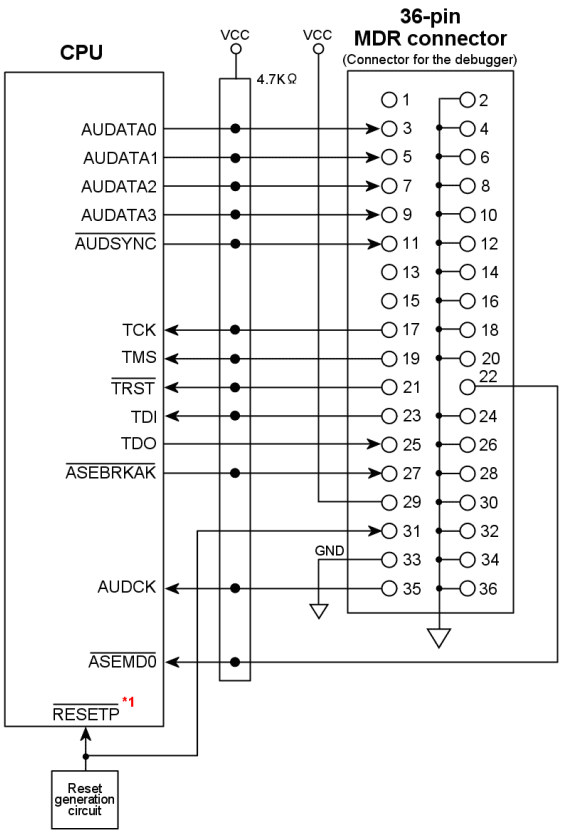
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

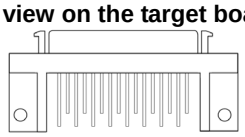
Target connection reference diagram



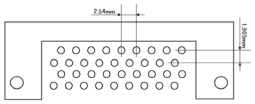
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

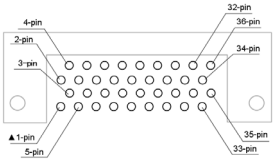
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7709S)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH3-DSP

SH7290(SH-Mobile1)
SH7294(SH-MobileJ)
SH7300(SH-MobileV)
SH7710
SH7712
SH7713
SH7720/SH7721
SH7727
SH7729
SH7729R

SH7290(SH-Mobile1)

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

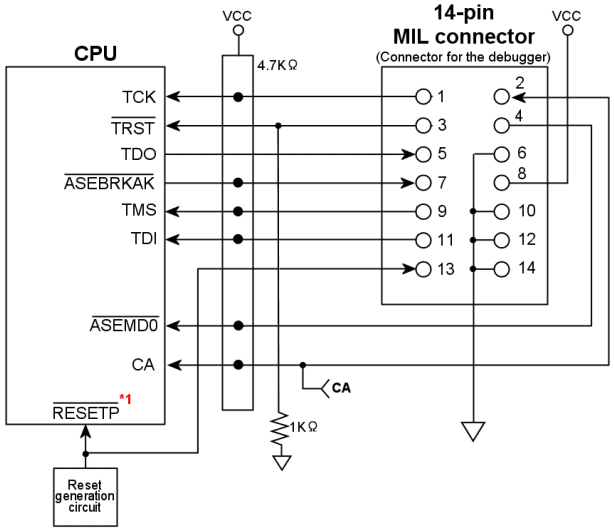
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			CSP-240	CSP-256				CSP-240	CSP-256
1	TCK	Input	H18	J18	2	CA	Output	M18	N20
3	$\overline{\text{TRST}}$	Input	J18	K20	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(M17)	(M18)
5	TDO	Output	T18	U21	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	U18	V20	8	VCC *3	Output		
9	TMS	Input	J19	K17	10	GND			
11	TDI	Input	H17	J21	12	GND			
13	$\overline{\text{RESETP}}$	Output	N16	N21	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

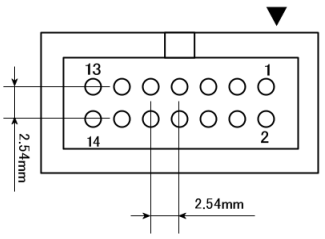
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

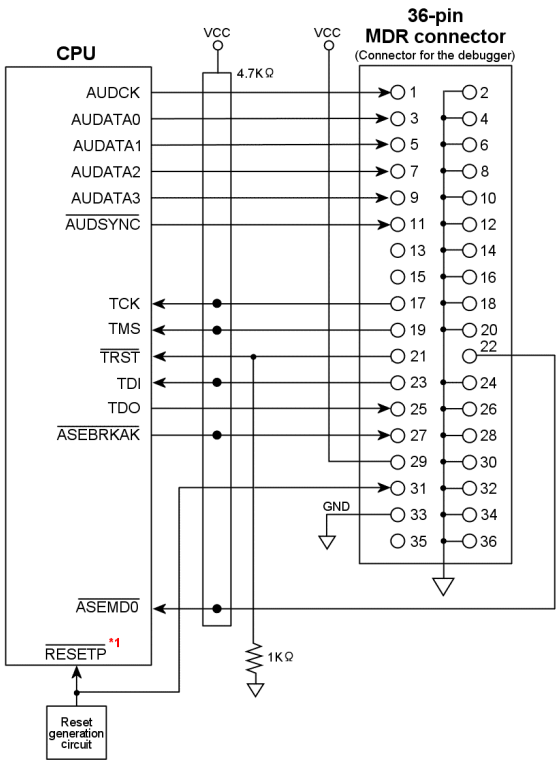
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			CSP-240	CSP-256				CSP-240	CSP-256
1	AUDCK	Output	R18	T21	2	GND			
3	AUDATA0	Output	J17	K21	4	GND			
5	AUDATA1	Output	K19	L17	6	GND			
7	AUDATA2	Output	K17	M17	8	GND			
9	AUDATA3	Output	K18	L21	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	T14	Y14	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	H18	J18	18	GND			
19	TMS	Input	J19	K17	20	GND			
21	$\overline{\text{TRST}}$	Input	J18	K20	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(M17)	(M18)
23	TDI	Input	H17	J21	24	GND			
25	TDO	Output	T18	U21	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	U18	V20	28	GND			
29	VCC *3 *4	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	N16	N21	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: In the target connection reference diagram, Pin No. 29 is VCC, however, CA pin can also be connected to Pin No. 29.
*4: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

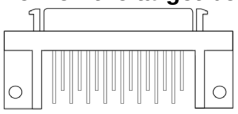
Target connection reference diagram



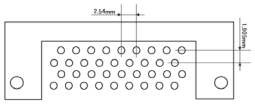
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

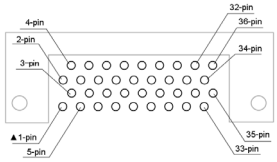
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7290(SH-Mobile1))

First Edition	Jun. 30, 2009	Initial edition

SH7294(SH-MobileJ)

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-225	Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-225
1	TCK	Input	C2	2	CA	Output	H18
3	$\overline{\text{TRST}}$	Input	E2	4	GND($\overline{\text{ASEMD0}}$)*2	(Input)	(J15)
5	TDO	Output	E1	6	GND		
7	$\overline{\text{ASEBRKAK}}$	Output	G4	8	VCC *3	Output	
9	TMS	Input	F4	10	GND		
11	TDI	Input	D2	12	GND		
13	$\overline{\text{RESETP}}$	Output	H15	14	GND		

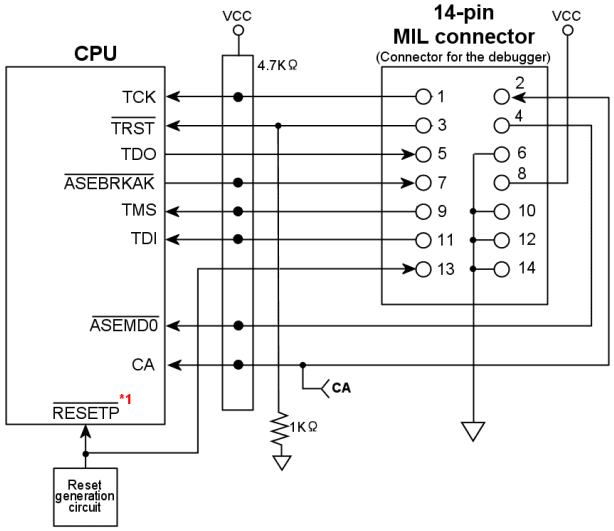
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

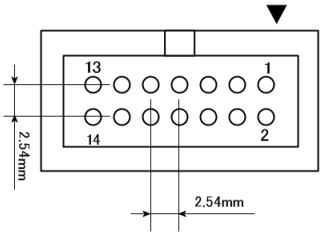
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

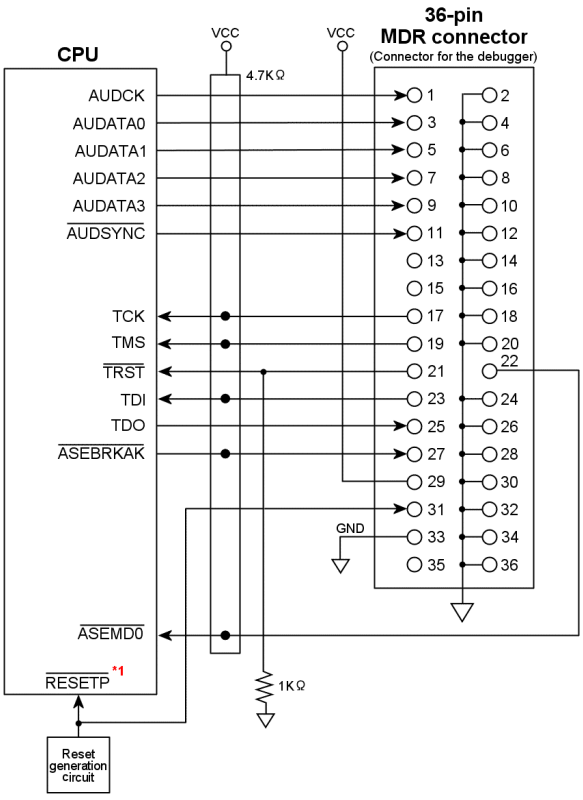
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-225	Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-225
1	AUDCK	Output	M18	2	GND		
3	AUDATA0	Output	J16	4	GND		
5	AUDATA1	Output	K18	6	GND		
7	AUDATA2	Output	K16	8	GND		
9	AUDATA3	Output	L18	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	J18	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	C2	18	GND		
19	TMS	Input	F4	20	GND		
21	$\overline{\text{TRST}}$	Input	E2	22	GND($\overline{\text{ASEMD0}}$)*2	(Input)	(J15)
23	TDI	Input	D2	24	GND		
25	TDO	Output	E1	26	GND		
27	$\overline{\text{ASEBRKAK}}$	Output	G4	28	GND		
29	VCC *3 *4	Output		30	GND		
31	$\overline{\text{RESETP}}$	Output	H15	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: In the target connection reference diagram, Pin No. 29 is VCC, however, CA pin can also be connected to Pin No. 29.
*4: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

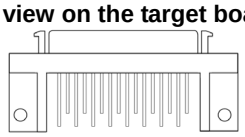
Target connection reference diagram



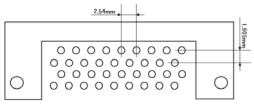
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

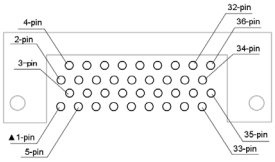
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7294(SH-MobileJ))

First Edition	Jun. 30, 2009	Initial edition

SH7300(SH-MobileV)

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-256	Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-256
1	TCK	Input	K20	2	CA	Output	J20
3	$\overline{\text{TRST}}$	Input	J17	4	GND($\overline{\text{ASEMD0}}$)*2	(Input)	(K21)
5	TDO	Output	J18	6	GND		
7	$\overline{\text{ASEBRKAK}}$	Output	N20	8	VCC *3	Output	
9	TMS	Input	J21	10	GND		
11	TDI	Input	K17	12	GND		
13	$\overline{\text{RESETP}}$	Output	H17	14	GND		

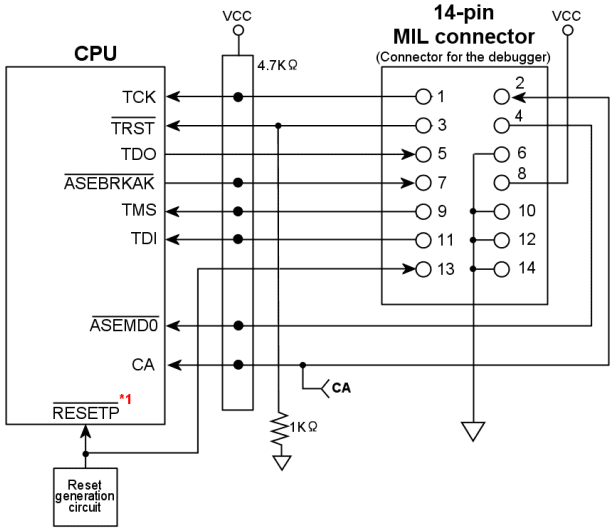
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

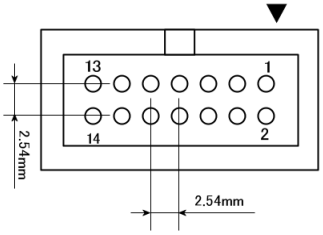
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

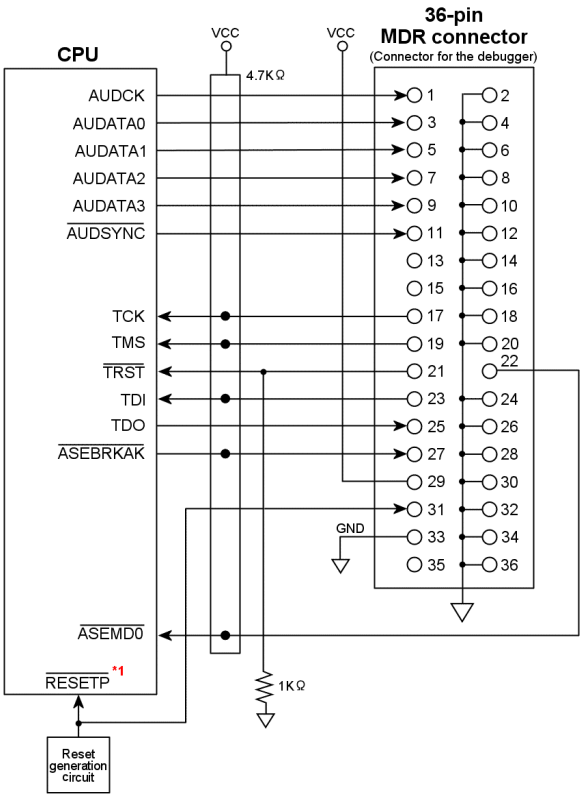
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-256	Pin No.	Signal	Input/ Output*1	CPU Pin No. CSP-256
1	AUDCK	Output	L20	2	GND		
3	AUDATA0	Output	L18	4	GND		
5	AUDATA1	Output	M20	6	GND		
7	AUDATA2	Output	N17	8	GND		
9	AUDATA3	Output	M21	10	GND		
11	$\overline{\text{AUDSYNC}}$	Output	P17	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	K20	18	GND		
19	TMS	Input	J21	20	GND		
21	$\overline{\text{TRST}}$	Input	J17	22	GND($\overline{\text{ASEMD0}}$)*2	(Input)	(K21)
23	TDI	Input	K17	24	GND		
25	TDO	Output	J18	26	GND		
27	$\overline{\text{ASEBRKAK}}$	Output	N20	28	GND		
29	VCC *3 *4	Output		30	GND		
31	$\overline{\text{RESETP}}$	Output	H17	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: In the target connection reference diagram, Pin No. 29 is VCC, however, CA pin can also be connected to Pin No. 29.
*4: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

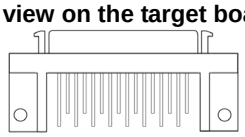
Target connection reference diagram



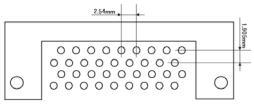
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

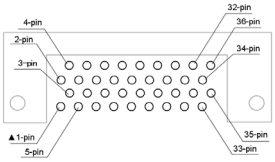
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7300(SH-MobileV))

First Edition	Jun. 30, 2009	Initial edition

SH7710

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

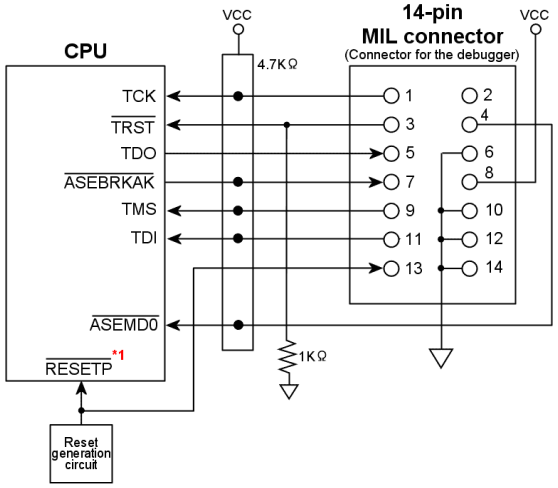
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A
1	TCK	Input	202	D16	2	N.C.			
3	$\overline{\text{TRST}}$	Input	201	A17	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(197)	(B16)
5	TDO	Output	200	C17	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	203	B15	8	VCC *3	Output		
9	TMS	Input	199	A18	10	GND			
11	TDI	Input	198	C16	12	GND			
13	$\overline{\text{RESETP}}$	Output	215	A13	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

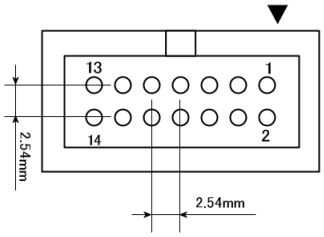
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A
1	AUDCK	Output	205	A16	2	GND			
3	AUDATA0	Output	213	A14	4	GND			
5	AUDATA1	Output	212	C13	6	GND			
7	AUDATA2	Output	211	B13	8	GND			
9	AUDATA3	Output	210	D14	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	204	C15	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	202	D16	18	GND			
19	TMS	Input	199	A18	20	GND			
21	$\overline{\text{TRST}}$	Input	201	A17	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(197)	(B16)
23	TDI	Input	198	C16	24	GND			
25	TDO	Output	200	C17	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	203	B15	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	215	A13	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

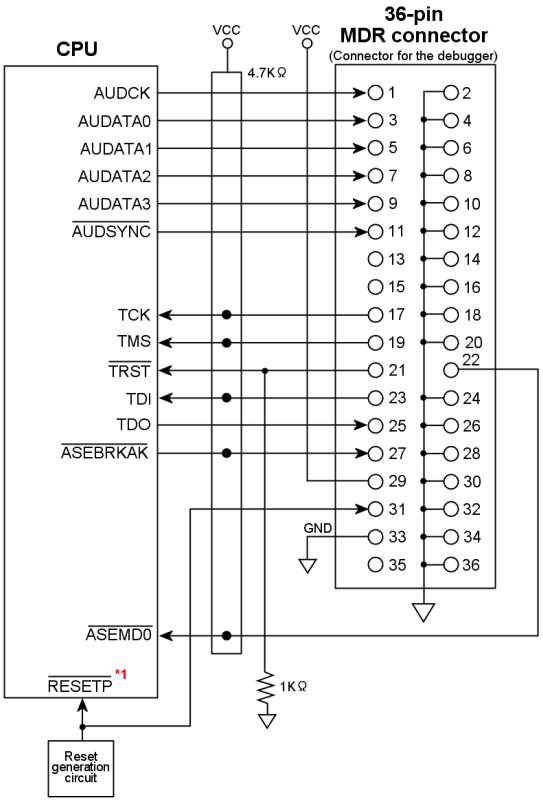
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

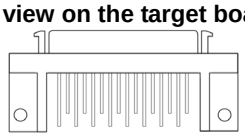
Target connection reference diagram



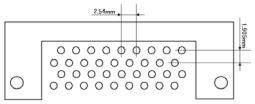
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

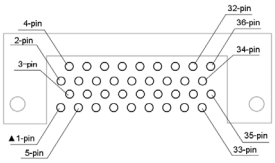
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7710)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7712

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

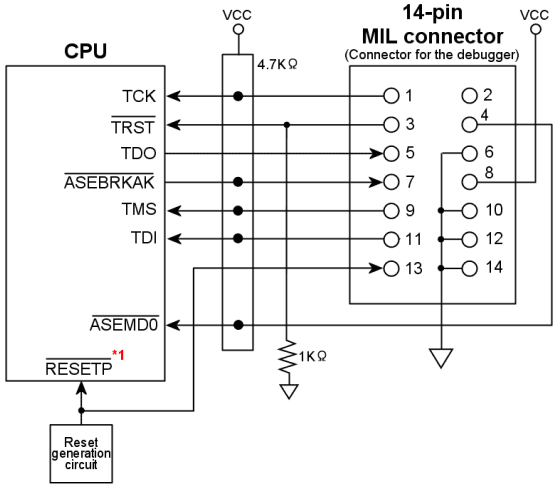
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A
1	TCK	Input	202	D16	2	N.C.			
3	$\overline{\text{TRST}}$	Input	201	A17	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(197)	(B16)
5	TDO	Output	200	C17	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	203	B15	8	VCC *3	Output		
9	TMS	Input	199	A18	10	GND			
11	TDI	Input	198	C16	12	GND			
13	$\overline{\text{RESETP}}$	Output	215	A13	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

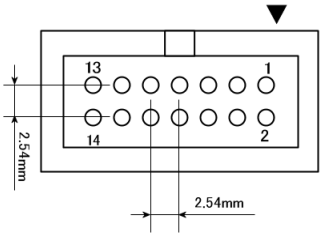
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PLBG0256 GA-A
1	AUDCK	Output	205	A16	2	GND			
3	AUDATA0	Output	213	A14	4	GND			
5	AUDATA1	Output	212	C13	6	GND			
7	AUDATA2	Output	211	B13	8	GND			
9	AUDATA3	Output	210	D14	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	204	C15	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	202	D16	18	GND			
19	TMS	Input	199	A18	20	GND			
21	$\overline{\text{TRST}}$	Input	201	A17	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(197)	(B16)
23	TDI	Input	198	C16	24	GND			
25	TDO	Output	200	C17	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	203	B15	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	215	A13	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

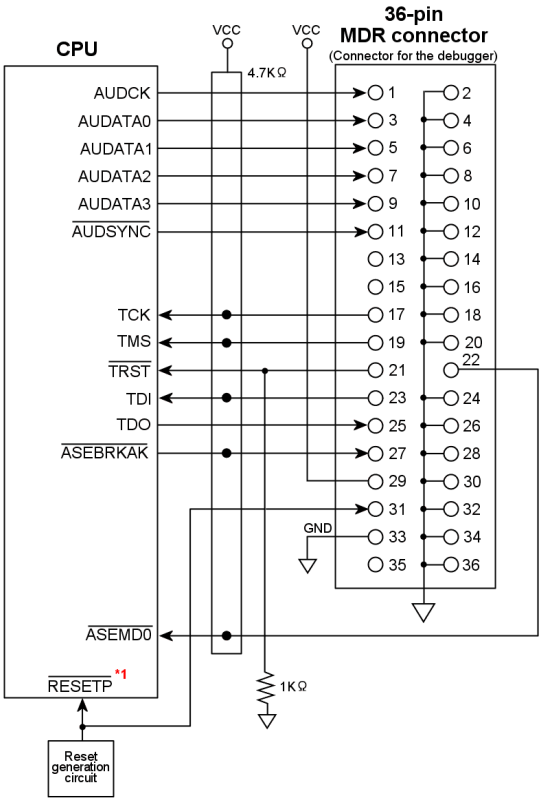
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

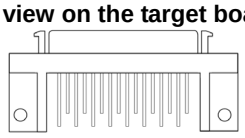
Target connection reference diagram



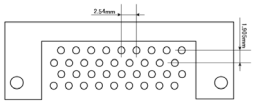
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

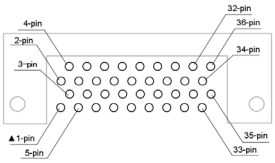
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7712)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7713

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

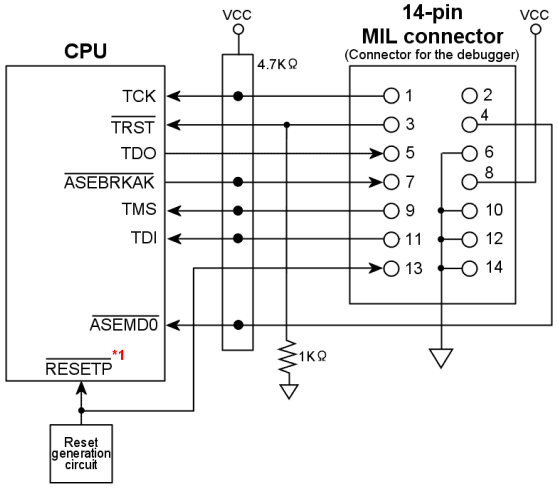
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PRQP0256 LA-B	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PRQP0256 LA-B
1	TCK	Input	202	D16	2	N.C.			
3	$\overline{\text{TRST}}$	Input	201	A17	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(197)	(B16)
5	TDO	Output	200	C17	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	203	B15	8	VCC *3	Output		
9	TMS	Input	199	A18	10	GND			
11	TDI	Input	198	C16	12	GND			
13	$\overline{\text{RESETP}}$	Output	215	A13	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

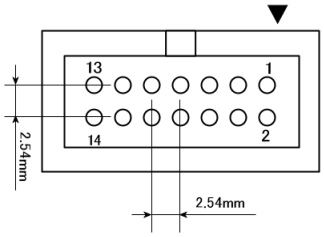
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PRQP0256 LA-B	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0256 LA-B	CPU Pin No. PRQP0256 LA-B
1	AUDCK	Output	205	A16	2	GND			
3	AUDATA0	Output	213	A14	4	GND			
5	AUDATA1	Output	212	C13	6	GND			
7	AUDATA2	Output	211	B13	8	GND			
9	AUDATA3	Output	210	D14	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	204	C15	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	202	D16	18	GND			
19	TMS	Input	199	A18	20	GND			
21	$\overline{\text{TRST}}$	Input	201	A17	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(197)	(B16)
23	TDI	Input	198	C16	24	GND			
25	TDO	Output	200	C17	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	203	B15	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	215	A13	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

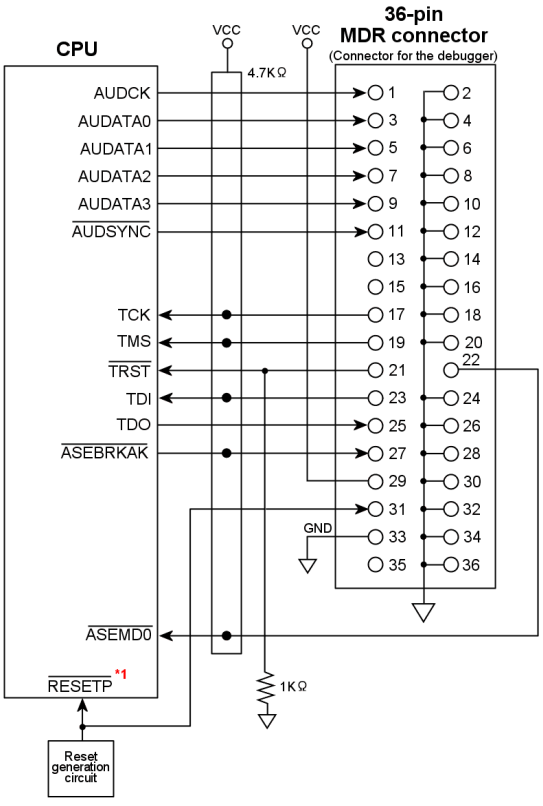
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

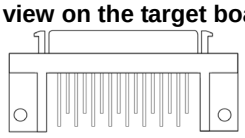
Target connection reference diagram



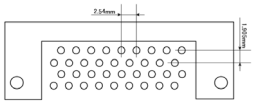
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

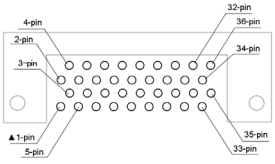
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7713)

First Edition	Jun. 30, 2009	Initial edition

SH7720/SH7721

Applicable products*1	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

***1: SH7721 is not supported by PALMiCE2-SH.**

MIL connector

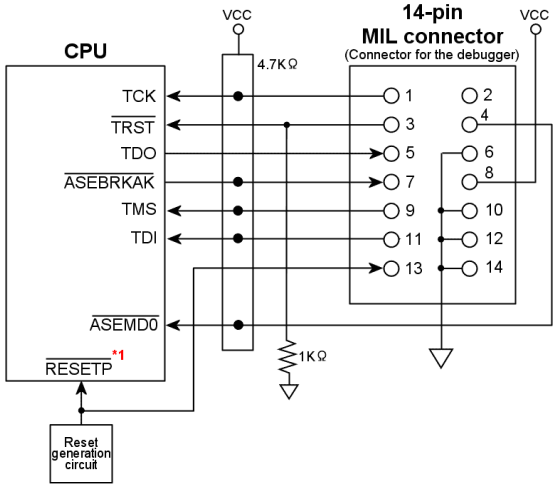
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0256 GA-A	CPU Pin No. PLBG0256 KA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0256 GA-A	CPU Pin No. PLBG0256 KA-A
1	TCK	Input	T18	T18	2	N.C.			
3	$\overline{\text{TRST}}$	Input	R19	R18	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(R18)	(R21)
5	TDO	Output	U20	W20	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	T20	V18	8	VCC *3	Output		
9	TMS	Input	T17	U20	10	GND			
11	TDI	Input	U18	T21	12	GND			
13	$\overline{\text{RESETP}}$	Output	V18	V17	14	GND			

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

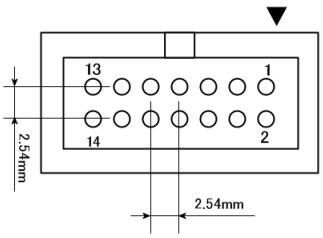
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0256 GA-A	CPU Pin No. PLBG0256 KA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0256 GA-A	CPU Pin No. PLBG0256 KA-A
1	AUDCK	Output	P19	P18	2	GND			
3	AUDATA0	Output	P18	R20	4	GND			
5	AUDATA1	Output	N19	N18	6	GND			
7	AUDATA2	Output	N18	P20	8	GND			
9	AUDATA3	Output	N20	R17	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	R17	T20	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	T18	T18	18	GND			
19	TMS	Input	T17	U20	20	GND			
21	$\overline{\text{TRST}}$	Input	R19	R18	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(R18)	(R21)
23	TDI	Input	U18	T21	24	GND			
25	TDO	Output	U20	W20	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	T20	V18	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	V18	V17	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

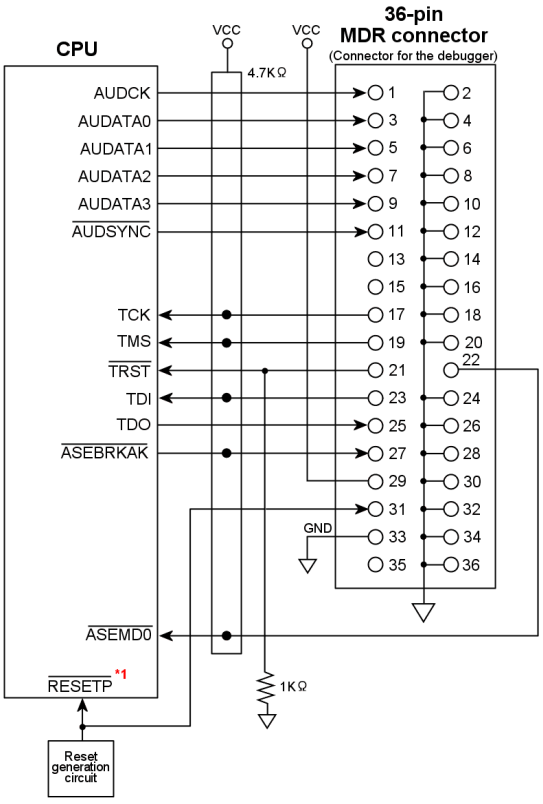
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

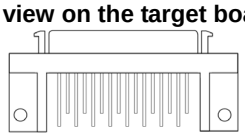
Target connection reference diagram



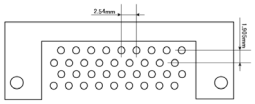
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

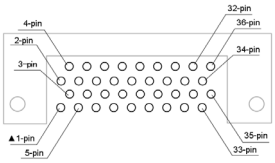
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7720/SH7721)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH. Also, added CPU SH7721.

SH7727

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

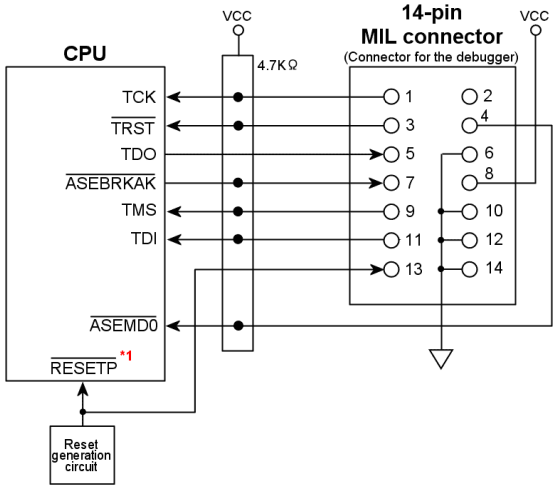
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0240 KC-B	CPU Pin No. PLBG0240 JA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0240 KC-B	CPU Pin No. PLBG0240 JA-A
1	TCK	Input	164	W7	2	N.C.			
3	$\overline{\text{TRST}}$	Input	160	W8	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(150)	(T10)
5	TDO	Output	143	U12	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	151	U10	8	VCC *3	Output		
9	TMS	Input	162	U7	10	GND			
11	TDI	Input	163	V7	12	GND			
13	$\overline{\text{RESETP}}$	Output	220	H1	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

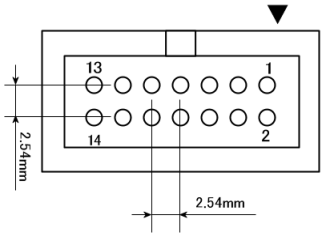
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0240 KC-B	CPU Pin No. PLBG0240 JA-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PRQP0240 KC-B	CPU Pin No. PLBG0240 JA-A
1	N.C.				2	GND			
3	AUDATA0	Output	158	U8	4	GND			
5	AUDATA1	Output	156	W9	6	GND			
7	AUDATA2	Output	154	T9	8	GND			
9	AUDATA3	Output	153	U9	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	104	N19	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	164	W7	18	GND			
19	TMS	Input	162	U7	20	GND			
21	$\overline{\text{TRST}}$	Input	160	W8	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(150)	(T10)
23	TDI	Input	163	V7	24	GND			
25	TDO	Output	143	U12	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	151	U10	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	220	H1	32	GND			
33	GND				34	GND			
35	AUDCK	Input	176	W3	36	GND			

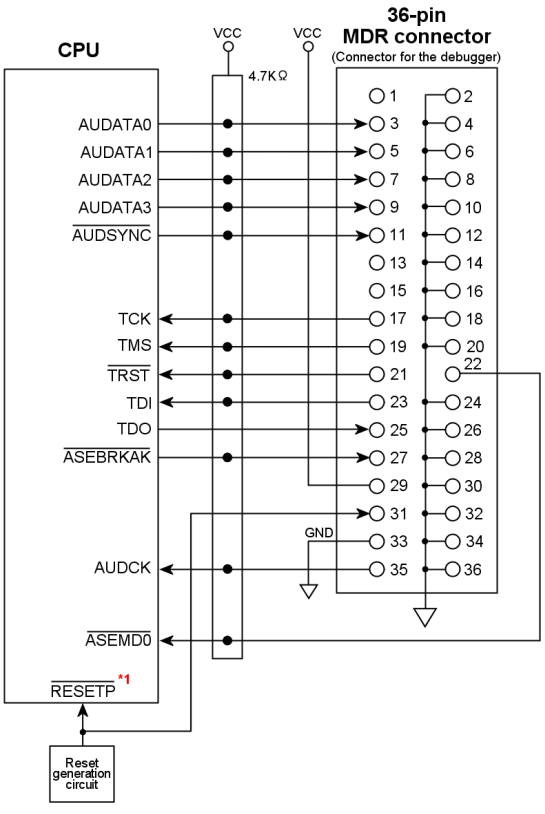
- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

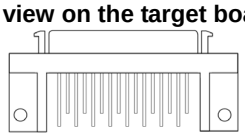
Target connection reference diagram



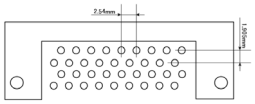
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

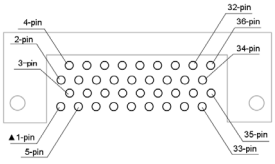
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7727)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7729

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

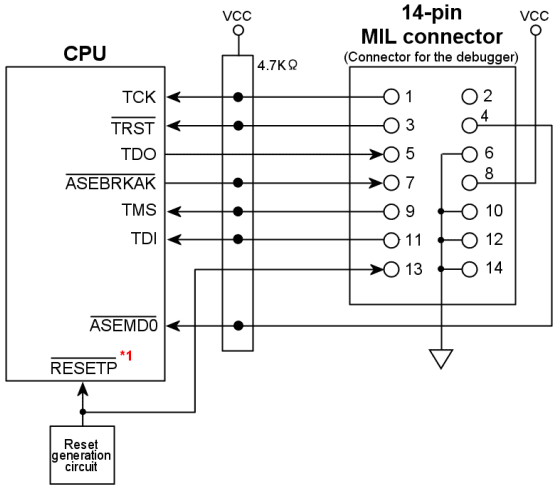
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-208C	TBT-216B				FP-208C	TBT-216B
1	TCK	Input	139	AH11	2	N.C.			
3	$\overline{\text{TRST}}$	Input	136	AJ13	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(127)	(AH17)
5	TDO	Output	120	AJ21	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	128	AJ17	8	VCC *3	Output		
9	TMS	Input	137	AH12	10	GND			
11	TDI	Input	138	AJ12	12	GND			
13	$\overline{\text{RESETP}}$	Output	193	K02	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

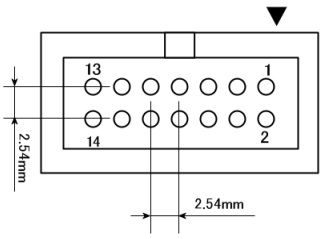
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-208C	TBT-216B				FP-208C	TBT-216B
1	N.C.				2	GND			
3	AUDATA0	Output	135	AH13	4	GND			
5	AUDATA1	Output	133	AH14	6	GND			
7	AUDATA2	Output	131	AH15	8	GND			
9	AUDATA3	Output	130	AJ16	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	94	AB29	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	139	AH11	18	GND			
19	TMS	Input	137	AH12	20	GND			
21	$\overline{\text{TRST}}$	Input	136	AJ13	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(127)	(AH17)
23	TDI	Input	138	AJ12	24	GND			
25	TDO	Output	120	AJ21	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	128	AJ17	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	193	K02	32	GND			
33	GND				34	GND			
35	AUDCK	Input	151	AH05	36	GND			

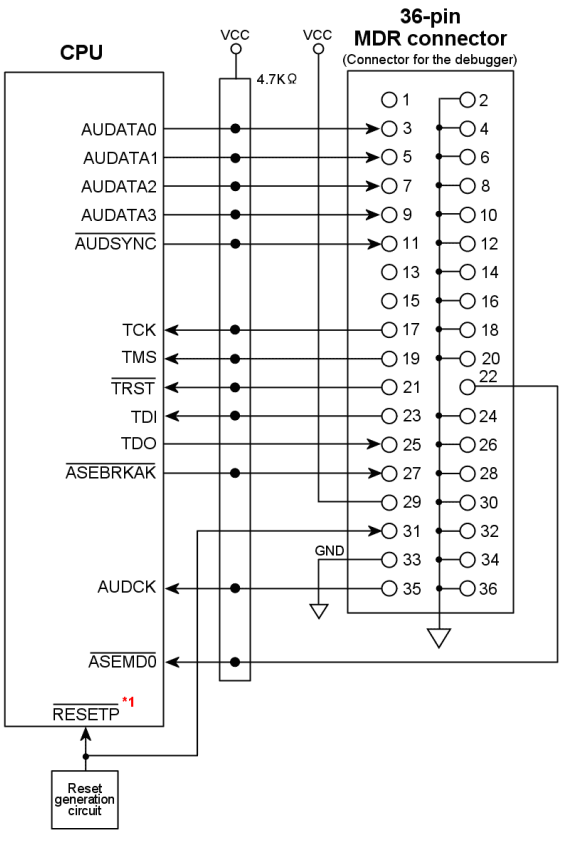
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

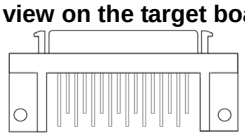
Target connection reference diagram



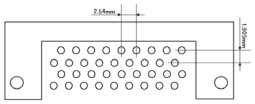
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

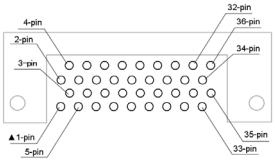
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7729)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7729R

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

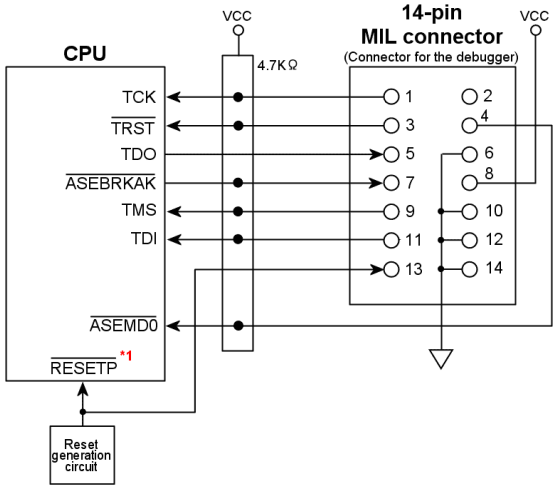
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-208C/E	BP-240A				FP-208C/E	BP-240A
1	TCK	Input	139	H18	2	N.C.			
3	$\overline{\text{TRST}}$	Input	136	J19	4	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(127)	(L19)
5	TDO	Output	120	N18	6	GND			
7	$\overline{\text{ASEBRKAK}}$	Output	128	L18	8	VCC *3	Output		
9	TMS	Input	137	H16	10	GND			
11	TDI	Input	138	H17	12	GND			
13	$\overline{\text{RESETP}}$	Output	193	C7	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 4 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

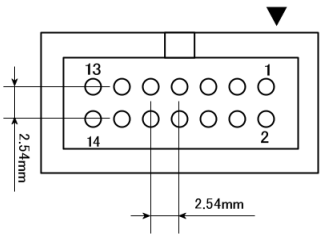
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.		Pin No.	Signal	Input/ Output*1	CPU Pin No.	
			FP-208C/E	BP-240A				FP-208C/E	BP-240A
1	N.C.				2	GND			
3	AUDATA0	Output	135	J18	4	GND			
5	AUDATA1	Output	133	K19	6	GND			
7	AUDATA2	Output	131	K18	8	GND			
9	AUDATA3	Output	130	L17	10	GND			
11	$\overline{\text{AUDSYNC}}$	Output	94	V14	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	139	H18	18	GND			
19	TMS	Input	137	H16	20	GND			
21	$\overline{\text{TRST}}$	Input	136	J19	22	GND ($\overline{\text{ASEMD0}}$)*2	(Input)	(127)	(L19)
23	TDI	Input	138	H17	24	GND			
25	TDO	Output	120	N18	26	GND			
27	$\overline{\text{ASEBRKAK}}$	Output	128	L18	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$	Output	193	C7	32	GND			
33	GND				34	GND			
35	AUDCK	Input	151	D16	36	GND			

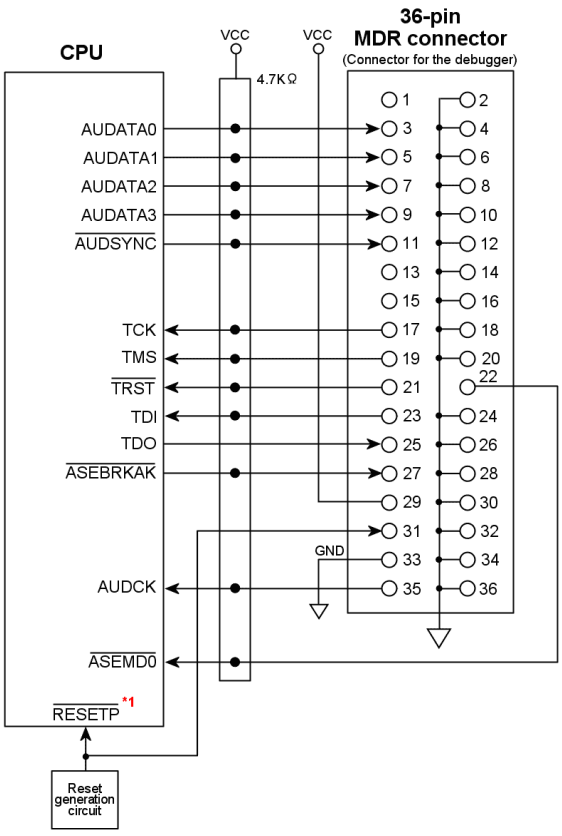
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, $\overline{\text{ASEMD0}}$ pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings $\overline{\text{ASEMD0}}$ pin to Low state when you connect $\overline{\text{ASEMD0}}$ signal to the connector for debugger.
If you do not connect $\overline{\text{ASEMD0}}$ signal to Pin No. 22 of the connector for debugger, the circuit that sets $\overline{\text{ASEMD0}}$ pin by switch circuit will do. However, in such case, do not connect $\overline{\text{ASEMD0}}$ pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

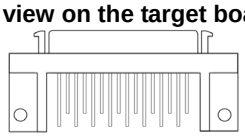
Target connection reference diagram



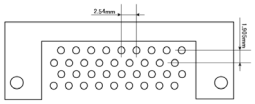
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

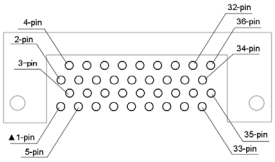
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7729R)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH4AL-DSP

SH7343(SH-Mobile3AS)
SH7354(SH-MobileL3V)
SH7722(SH-MobileR)

SH7343(SH-Mobile3AS)

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

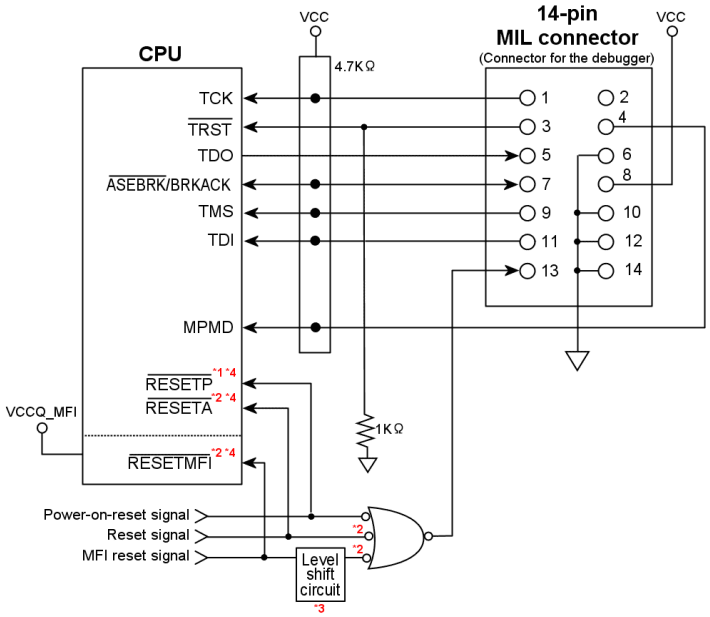
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-LFBGA1212 -409	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-LFBGA1212 -409
1	TCK	Input	AB15	2	N.C.		
3	$\overline{\text{TRST}}$	Input	W14	4	GND(MPMD)*2	(Input)	(AB13)
5	TDO	Output	Y14	6	GND		
7	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	AA13	8	VCC *3	Output	
9	TMS	Input	W15	10	GND		
11	TDI	Input	V15	12	GND		
13	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4 /$\overline{\text{RESETMFI}}$*4	Output Output Output	V16 AB17 E11	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$, $\overline{\text{RESETA}}$, and $\overline{\text{RESETMFI}}$, connect them as required with reference to the target connection reference diagram.

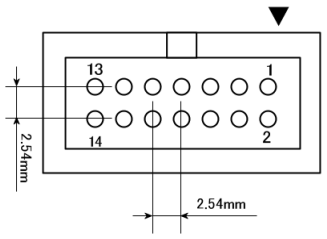
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$ or $\overline{\text{RESETMFI}}$.
*2: If you connect neither $\overline{\text{RESETA}}$or $\overline{\text{RESETMFI}}$, fix it to High.
*3: If you are using VccQ MFI at 1.8V, level shift circuit shown in the target connection reference diagram is required to adjust the signal level.
*4: The signal, which is connected to Pin No.13 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin, $\overline{\text{RESETA}}$ pin, and $\overline{\text{RESETMFI}}$ pin of CPU.

MDR connector

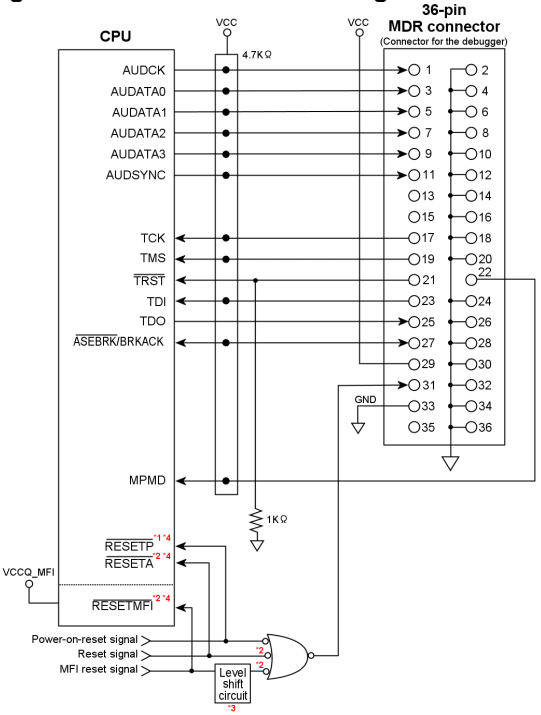
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-LFBGA1212 -409	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-LFBGA1212 -409
1	AUDCK	Output	Y13	2	GND		
3	AUDATA0	Output	AA14	4	GND		
5	AUDATA1	Output	V14	6	GND		
7	AUDATA2	Output	AB14	8	GND		
9	AUDATA3	Output	W13	10	GND		
11	AUDSYNC	Output	V13	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	AB15	18	GND		
19	TMS	Input	W15	20	GND		
21	$\overline{\text{TRST}}$	Input	W14	22	GND(MPMD)*2	(Input)	(AB13)
23	TDI	Input	V15	24	GND		
25	TDO	Output	Y14	26	GND		
27	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	AA13	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4 /$\overline{\text{RESETMFI}}$*4	Output Output Output	V16 AB17 E11	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$, $\overline{\text{RESETA}}$, and $\overline{\text{RESETMFI}}$, connect them as required with reference to the target connection reference diagram.

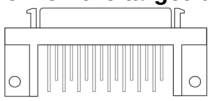
Target connection reference diagram



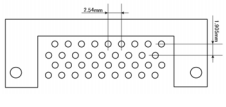
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

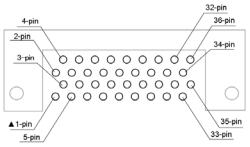
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$ or $\overline{\text{RESETMFI}}$.
*2: If you connect neither $\overline{\text{RESETA}}$or $\overline{\text{RESETMFI}}$, fix it to High.
*3: If you are using VccQ MFI at 1.8V, level shift circuit shown in the target connection reference diagram is required to adjust the signal level.
*4: The signal, which is connected to Pin No.31 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin, $\overline{\text{RESETA}}$ pin, and $\overline{\text{RESETMFI}}$ pin of CPU.

Document change history (SH7343(SH-Mobile3AS))

First Edition	Jun. 30, 2009	Initial edition

SH7354(SH-MobileL3V)

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

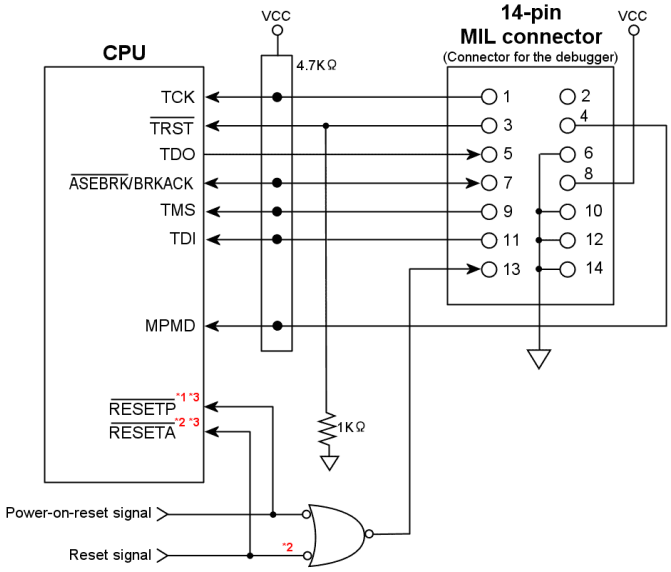
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0281KE-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0281KE-A
1	TCK	Input	V3	2	N.C.		
3	$\overline{\text{TRST}}$	Input	T5	4	GND(MPMD)*2	(Input)	(Y8)
5	TDO	Output	V4	6	GND		
7	$\overline{\text{ASEBRK}}$ /BRKACK	Input/Output	W6	8	VCC *3	Output	
9	TMS	Input	U4	10	GND		
11	TDI	Input	W3	12	GND		
13	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4	Output Output	T3 P4	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$, and $\overline{\text{RESETA}}$, connect them as required with reference to the target connection reference diagram.

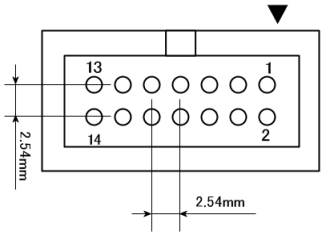
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$.
*2: If you do not connect $\overline{\text{RESETA}}$, fix it to High.
*3: The signal, which is connected to Pin No.13 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$pin and $\overline{\text{RESETA}}$pin of CPU.

MDR connector

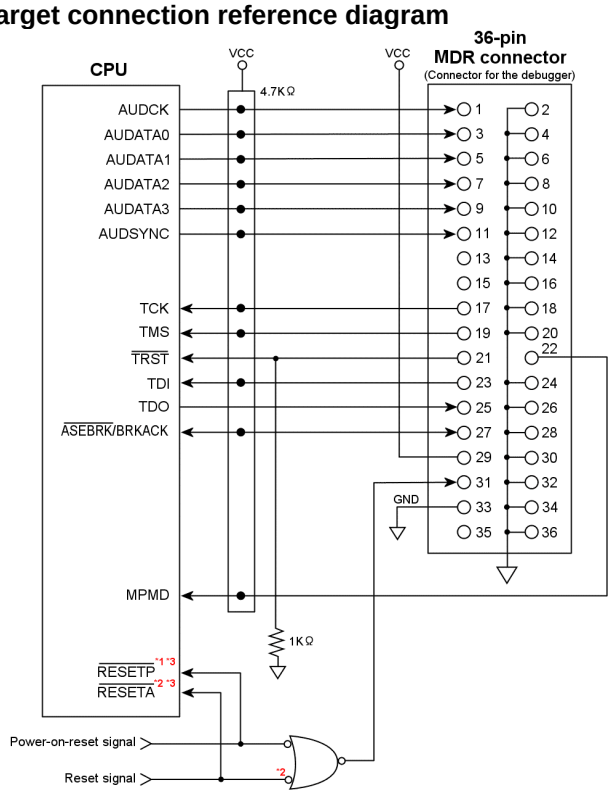
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0281KE-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLBG0281KE-A
1	AUDCK	Output	W5	2	GND		
3	AUDATA0	Output	W4	4	GND		
5	AUDATA1	Output	V5	6	GND		
7	AUDATA2	Output	U5	8	GND		
9	AUDATA3	Output	U6	10	GND		
11	AUDSYNC	Output	V6	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	V3	18	GND		
19	TMS	Input	U4	20	GND		
21	$\overline{\text{TRST}}$	Input	T5	22	GND(MPMD)*2	(Input)	(Y8)
23	TDI	Input	W3	24	GND		
25	TDO	Output	V4	26	GND		
27	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	W6	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4	Output Output	T3 P4	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$ and $\overline{\text{RESETA}}$, connect them as required with reference to the target connection reference diagram.

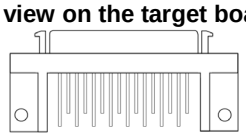
Target connection reference diagram



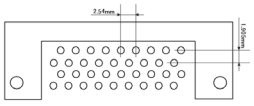
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

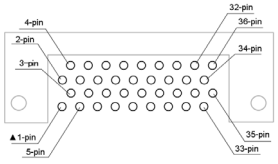
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$.
*2: If you do not connect $\overline{\text{RESETA}}$, fix it to High.
*3: The signal, which is connected to Pin No.31 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$pin and $\overline{\text{RESETA}}$pin of CPU.

Document change history (SH7354(SH-MobileL3V))

First Edition	Jun. 30, 2009	Initial edition

SH7722(SH-MobileR)

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

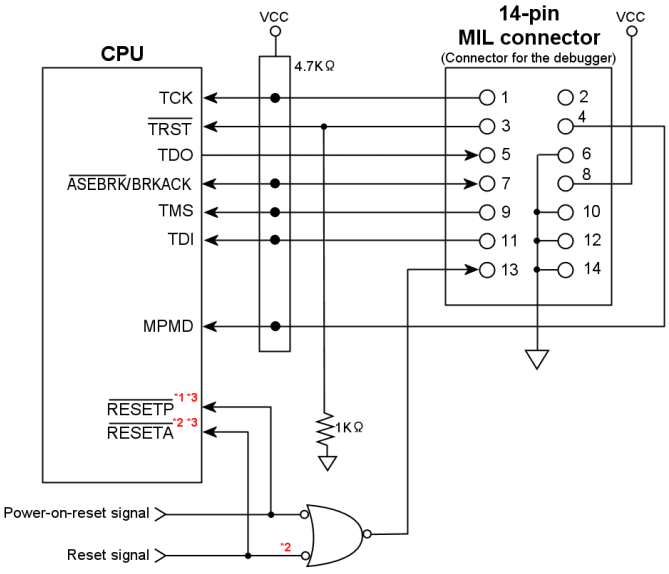
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. 417pin LFBGA	CPU Pin No. 449pin BGA	Pin No.	Signal	Input/ Output*1	CPU Pin No. 417pin LFBGA	CPU Pin No. 449pin BGA
1	TCK	Input	A7	A7	2	N.C.			
3	$\overline{\text{TRST}}$	Input	A6	C7	4	GND(MPMD)*2	(Input)	(C4)	(C5)
5	TDO	Output	C6	D8	6	GND			
7	$\overline{\text{ASEBRK}}$ /BRKACK	Input/Output	D4	D6	8	VCC *3	Output		
9	TMS	Input	D6	D9	10	GND			
11	TDI	Input	B6	B7	12	GND			
13	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4	Output Output	B8 D8	B9 C10	14	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$, and $\overline{\text{RESETA}}$, connect them as required with reference to the target connection reference diagram.

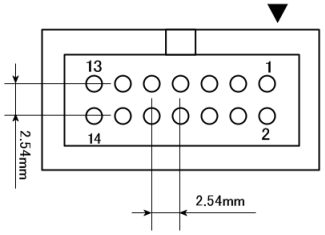
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$.
*2: If you do not connect $\overline{\text{RESETA}}$, fix it to High.
*3: The signal, which is connected to Pin No.13 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$pin and $\overline{\text{RESETA}}$pin of CPU.

MDR connector

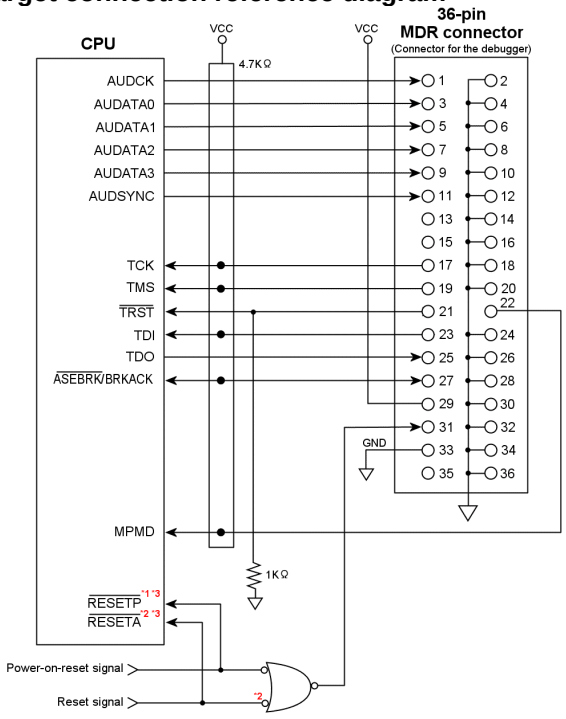
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. 417pin LFBGA	CPU Pin No. 449pin BGA	Pin No.	Signal	Input/ Output*1	CPU Pin No. 417pin LFBGA	CPU Pin No. 449pin BGA
1	AUDCK	Output	B5	A6	2	GND			
3	AUDATA0	Output	A5	B6	4	GND			
5	AUDATA1	Output	D5	D7	6	GND			
7	AUDATA2	Output	B4	C6	8	GND			
9	AUDATA3	Output	C5	A5	10	GND			
11	AUDSYNC	Output	A4	B5	12	GND			
13	N.C.				14	GND			
15	N.C.				16	GND			
17	TCK	Input	A7	A7	18	GND			
19	TMS	Input	D6	D9	20	GND			
21	$\overline{\text{TRST}}$	Input	A6	C7	22	GND(MPMD)*2	(Input)	(C4)	(C5)
23	TDI	Input	B6	B7	24	GND			
25	TDO	Output	C6	D8	26	GND			
27	$\overline{\text{ASEBRK}}$ /BRKACK	Input/Output	D4	D6	28	GND			
29	VCC *3	Output			30	GND			
31	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4	Output Output	B8 D8	B9 C10	32	GND			
33	GND				34	GND			
35	N.C.				36	GND			

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$ and $\overline{\text{RESETA}}$, connect them as required with reference to the target connection reference diagram.

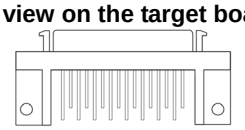
Target connection reference diagram



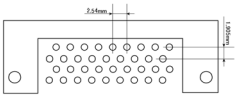
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

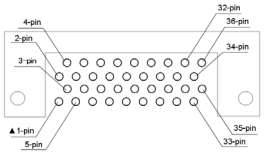
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$.
*2: If you do not connect $\overline{\text{RESETA}}$, fix it to High.
*3: The signal, which is connected to Pin No.31 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$pin and $\overline{\text{RESETA}}$pin of CPU.

Document change history (SH7722(SH-MobileR))

First Edition	Jun. 30, 2009	Initial edition

SH-4

SH7750R/SH7750S
SH7751/SH7751R
SH7760

SH7750R/SH7750S

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connector (Connector for debugger)	MIL connector (14-pin design)

MIL connector

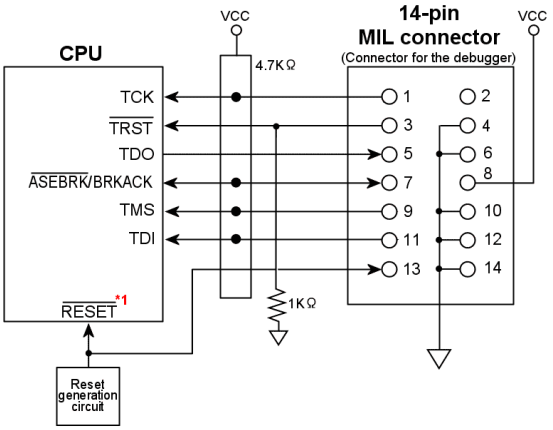
Signals

Pin No.	Signal	Input/ Output *1	CPU Pin No.				Pin No.	Signal	Input/ Output *1	CPU Pin No.			
			SH7750R/50S		SH7750S	SH7750R				SH7750R/50S		SH7750S	SH7750R
			BGA-256	QFP-2008	CSP-264	BGA-292				BGA-256	QFP-2008	CSP-264	BGA-292
1	TCK	Input	A5	198	C6	A6	2	N.C.					
3	$\overline{\text{TRST}}$	Input	C4	200	A5	B5	4	GND					
5	TDO	Output	A6	194	A6	C6	6	GND					
7	$\overline{\text{ASEBRK}}$/ BRKACK	Input/ Output	B7	193	E6	A7	8	VCC *2	Output				
9	TMS	Input	B6	197	E5	B6	10	GND					
11	TDI	Input	B5	199	D6	C5	12	GND					
13	$\overline{\text{RESET}}$	Output	B1	2	B1	B1	14	GND					

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

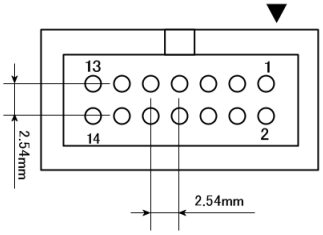
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESET}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESET}}$ pin of CPU.

Document change history (SH7750R/SH7750S)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Dec. 12, 2008	**Added a package to the table of Signals.** BGA-292
Third Edition	Jun. 30, 2009	Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.

SH7751/SH7751R

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

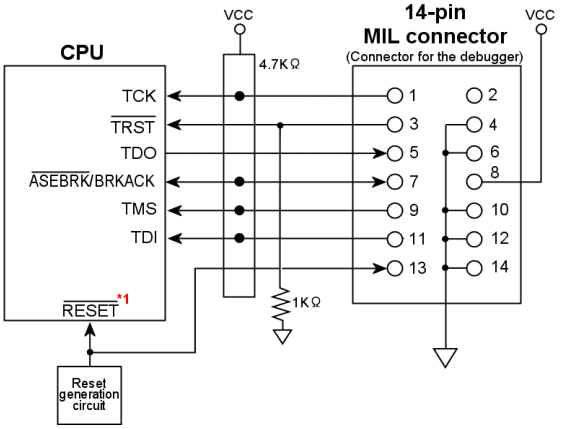
Signals

Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7751/51R QFP-256	CPU Pin No. SH7751/51R BGA-256	CPU Pin No. SH7751R BGA-292	Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7751/51R QFP-256	CPU Pin No. SH7751/51R BGA-256	CPU Pin No. SH7751R BGA-292
1	TCK	Input	2	C4	B2	2	N.C.				
3	$\overline{\text{TRST}}$	Input	199	C16	B17	4	GND				
5	TDO	Output	246	B4	C4	6	GND				
7	$\overline{\text{ASEBRK}}$/ BRKACK	Input/ Output	245	D5	B5	8	VCC *2	Output			
9	TMS	Input	1	B3	B1	10	GND				
11	TDI	Input	5	D4	C1	12	GND				
13	$\overline{\text{RESET}}$	Output	198	A17	A17	14	GND				

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

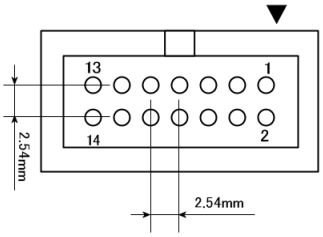
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESET}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESET}}$ pin of CPU.

MDR connector

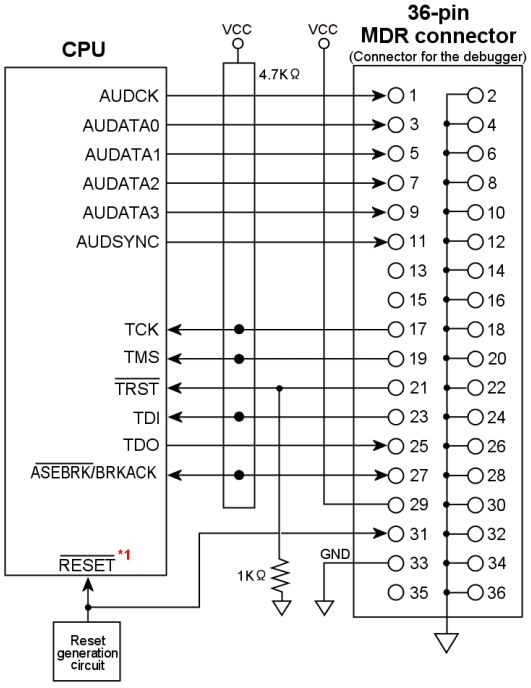
Signals

Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7751/51R QFP-256	CPU Pin No. SH7751/51R BGA-256	CPU Pin No. SH7751R BGA-292	Pin No.	Signal	Input/ Output *1	CPU Pin No. SH7751/51R QFP-256	CPU Pin No. SH7751/51R BGA-256	CPU Pin No. SH7751/51R BGA-292
1	AUDCK	Output	220	A11	B11	2	GND				
3	AUDATA0	Output	223	C10	A10	4	GND				
5	AUDATA1	Output	224	A10	B10	6	GND				
7	AUDATA2	Output	227	B9	C10	8	GND				
9	AUDATA3	Output	228	D9	A9	10	GND				
11	AUDSYNC	Output	219	B12	A11	12	GND				
13	N.C.					14	GND				
15	N.C.					16	GND				
17	TCK	Input	2	C4	B2	18	GND				
19	TMS	Input	1	B3	B1	20	GND				
21	$\overline{\text{TRST}}$	Input	199	C16	B17	22	GND				
23	TDI	Input	5	D4	C1	24	GND				
25	TDO	Output	246	B4	C4	26	GND				
27	$\overline{\text{ASEBRK}}$/ BRKACK	Input/ Output	245	D5	B5	28	GND				
29	VCC *2	Output				30	GND				
31	$\overline{\text{RESET}}$	Output	198	A17	A17	32	GND				
33	GND					34	GND				
35	N.C.					36	GND				

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

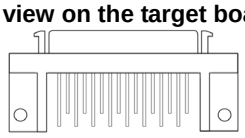
Target connection reference diagram



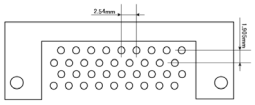
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

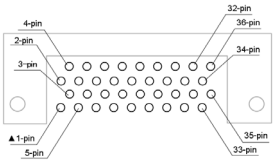
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESET}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESET}}$ pin of CPU.

Document change history (SH7751/SH7751R)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Dec. 12, 2008	**Added a package to the table of Signals.** BGA-292
Third Edition	Jun. 30, 2009	・ **Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.** ・ **Changed the descriptions of AUDSYNC signal regarding the following CPUs.** They had been written in negative logic, however, the descriptions were changed to positive logic so that they conform to the descriptions in the hardware manual published by Renesas Technology Corp..

SH7760

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

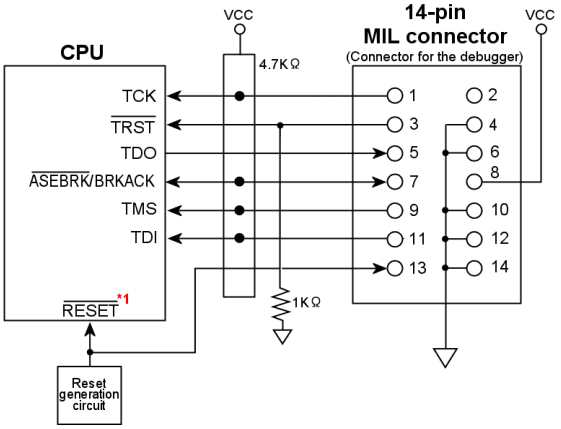
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-LBGA2121-256	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-LBGA2121-256
1	TCK	Input	C15	2	N.C.		
3	$\overline{\text{TRST}}$	Input	D10	4	GND		
5	TDO	Output	C12	6	GND		
7	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	C8	8	VCC *2	Output	
9	TMS	Input	C10	10	GND		
11	TDI	Input	D12	12	GND		
13	$\overline{\text{RESET}}$	Output	B1	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

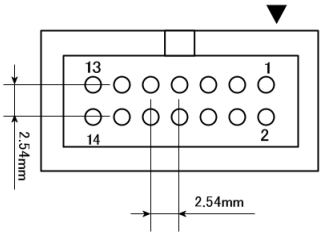
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESET}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESET}}$ pin of CPU.

MDR connector

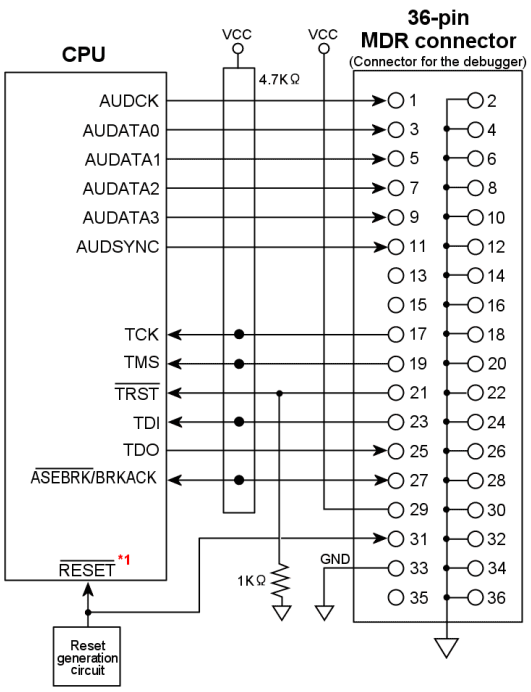
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 P-LBGA2121-256	Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 P-LBGA2121-256
1	AUDCK	Output	H19/P19	2	GND		
3	AUDATA0	Output	K19/T19	4	GND		
5	AUDATA1	Output	K20/T20	6	GND		
7	AUDATA2	Output	K19/R19	8	GND		
9	AUDATA3	Output	J20/R20	10	GND		
11	AUDSYNC	Output	H20/P20	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	C15	18	GND		
19	TMS	Input	C10	20	GND		
21	$\overline{\text{TRST}}$	Input	D10	22	GND		
23	TDI	Input	D12	24	GND		
25	TDO	Output	C12	26	GND		
27	$\overline{\text{ASEBRK}}$ /BRKACK	Input/Output	C8	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RESET}}$	Output	B1	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: 2 routings of AUD ports are available. Choose either of them.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

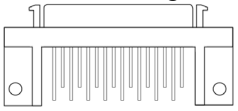
Target connection reference diagram



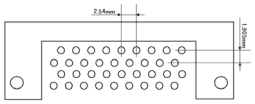
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

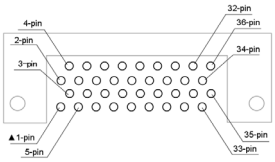
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESET}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESET}}$ pin of CPU.

Document change history (SH7760)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	・ **Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.** ・ **Changed the descriptions of AUDSYNC signal regarding the following CPUs.** They had been written in negative logic, however, the descriptions were changed to positive logic so that they conform to the descriptions in the hardware manual published by Renesas Technology Corp..

SH-4A

SH7723(SH-MobileR2)
SH7730
SH7763
SH7764
SH7770
SH7774
SH7780
SH7781
SH7785

SH7723(SH-MobileR2)

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

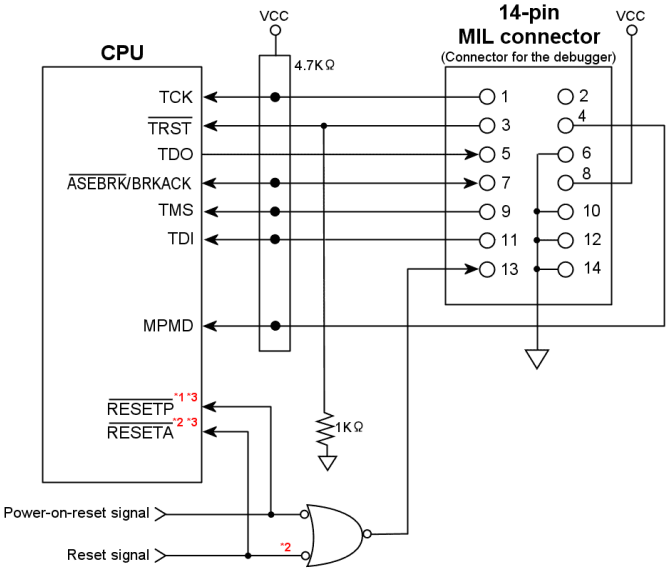
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449
1	TCK	Input	B16	2	N.C.		
3	$\overline{\text{TRST}}$	Input	A15	4	GND(MPMD)*2	(Input)	(B13)
5	TDO	Output	B15	6	GND		
7	$\overline{\text{ASEBRK}}$ /BRKACK	Input/Output	D12	8	VCC *3	Output	
9	TMS	Input	C15	10	GND		
11	TDI	Input	A16	12	GND		
13	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4	Output Output	B17 B18	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$, and $\overline{\text{RESETA}}$, connect them as required with reference to the target connection reference diagram.

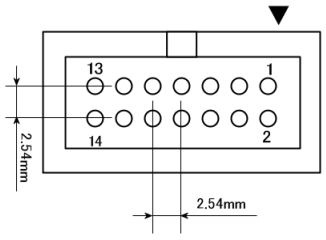
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$.
*2: If you do not connect $\overline{\text{RESETA}}$, fix it to High.
*3: The signal, which is connected to Pin No.13 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$pin and $\overline{\text{RESETA}}$pin of CPU.

MDR connector

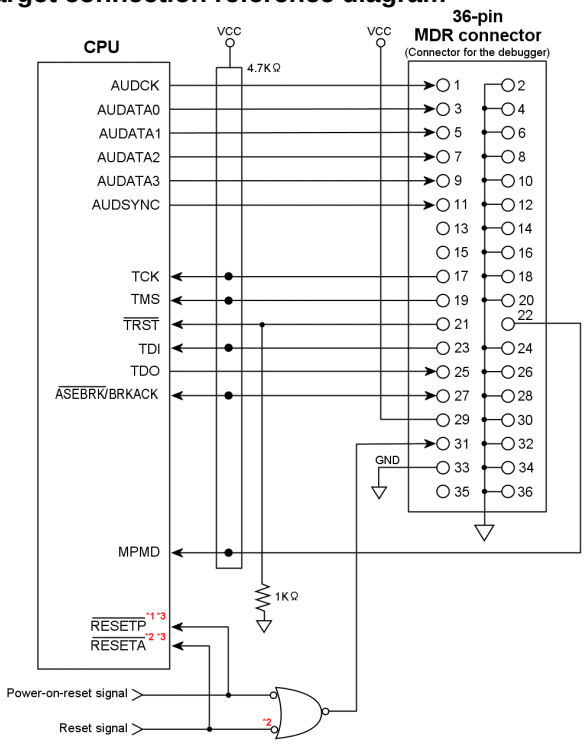
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449
1	AUDCK	Output	D14	2	GND		
3	AUDATA0	Output	C13	4	GND		
5	AUDATA1	Output	D13	6	GND		
7	AUDATA2	Output	A14	8	GND		
9	AUDATA3	Output	B14	10	GND		
11	AUDSYNC	Output	C14	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	B16	18	GND		
19	TMS	Input	C15	20	GND		
21	$\overline{\text{TRST}}$	Input	A15	22	GND(MPMD)*2	(Input)	(B13)
23	TDI	Input	A16	24	GND		
25	TDO	Output	B15	26	GND		
27	$\overline{\text{ASEBRK}}$ /BRKACK	Input/Output	D12	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RESETP}}$*4 /$\overline{\text{RESETA}}$*4	Output Output	B17 B18	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

- For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*4: As for $\overline{\text{RESETP}}$ and $\overline{\text{RESETA}}$, connect them as required with reference to the target connection reference diagram.

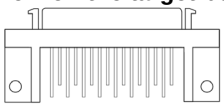
Target connection reference diagram



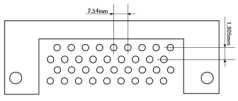
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

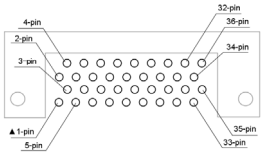
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$.
*2: If you do not connect $\overline{\text{RESETA}}$, fix it to High.
*3: The signal, which is connected to Pin No.31 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$pin and $\overline{\text{RESETA}}$pin of CPU.

Mictor connector

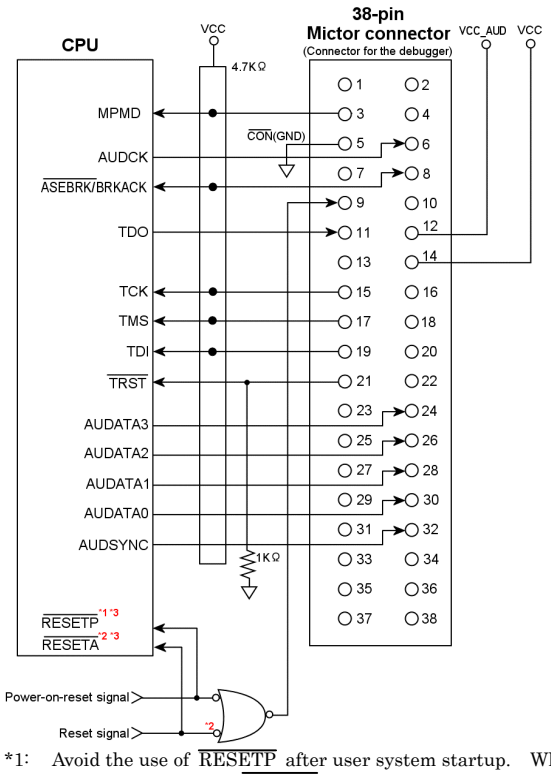
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449
1	N.C.			2	N.C.		
3	GND (MPMD) *2	(Input)	(B13)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *6	(Output)		6	AUDCK	Output	D14
7	N.C.			8	$\overline{\text{ASEBRK}}$ /BRKACK	Input/Output	D12
9	$\overline{\text{RESETP}}$*5 /$\overline{\text{RESETA}}$*5	Output Output	B17 B18	10	N.C.		
11	TDO	Output	B15	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	B16	16	N.C.		
17	TMS	Input	C15	18	N.C.		
19	TDI	Input	A16	20	N.C.		
21	$\overline{\text{TRST}}$	Input	A15	22	N.C.		
23	N.C.			24	AUDATA3	Output	B14
25	N.C.			26	AUDATA2	Output	A14
27	N.C.			28	AUDATA1	Output	D13
29	N.C.			30	AUDATA0	Output	C13
31	N.C.			32	AUDSYNC	Output	C14
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 3 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*5: As for $\overline{\text{RESETP}}$ and $\overline{\text{RESETA}}$, connect them as required with reference to the target connection reference diagram.
*6: By detection of GND on the target system side, whether the target system is connected or not is determined.

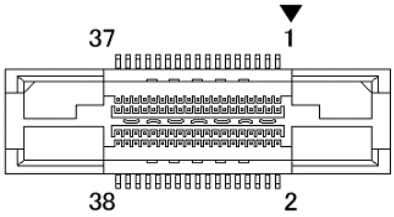
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: Avoid the use of $\overline{\text{RESETP}}$ after user system startup. When performing debugging with reset signal, use $\overline{\text{RESETA}}$.
*2: If you do not connect $\overline{\text{RESETA}}$, fix it to High.
*3: The signal, which is connected to Pin No.9 of the connector for debugger, is the signal that the debugger uses for monitoring the state of $\overline{\text{RESETP}}$pin and $\overline{\text{RESETA}}$pin of CPU.

Document change history (SH7723(SH-MobileR2))

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7730

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

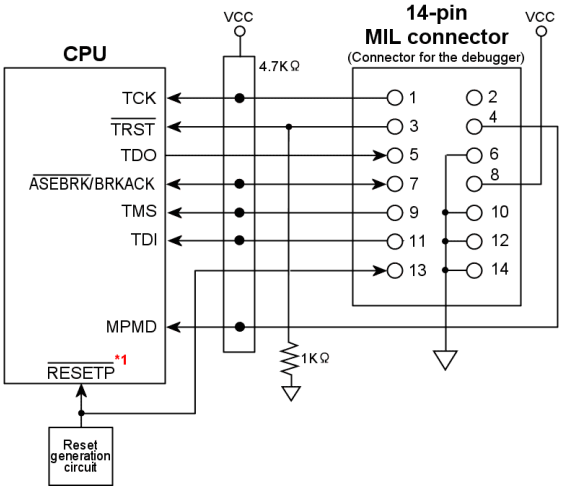
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KB-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KB-A
1	TCK	Input	139	2	N.C.		
3	$\overline{\text{TRST}}$	Input	136	4	GND (MPMD) *2	(Input)	(127)
5	TDO	Output	120	6	GND		
7	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	128	8	VCC *3	Output	
9	TMS	Input	137	10	GND		
11	TDI	Input	138	12	GND		
13	$\overline{\text{RESETP}}$	Output	193	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

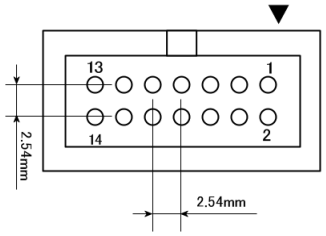
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

MDR connector

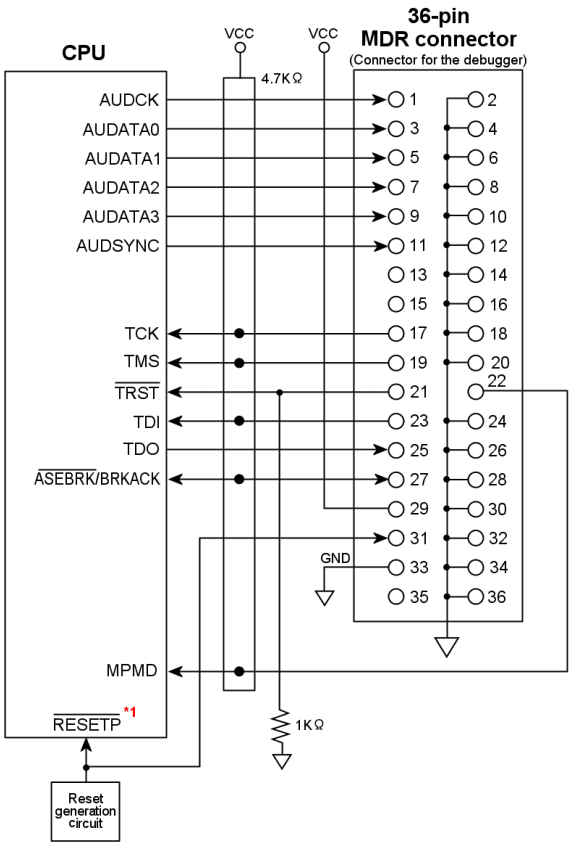
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KB-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KB-A
1	AUDCK	Output	124	2	GND		
3	AUDATA0	Output	135	4	GND		
5	AUDATA1	Output	133	6	GND		
7	AUDATA2	Output	131	8	GND		
9	AUDATA3	Output	130	10	GND		
11	AUDSYNC	Output	129	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	139	18	GND		
19	TMS	Input	137	20	GND		
21	$\overline{\text{TRST}}$	Input	136	22	GND (MPMD) *2	(Input)	(127)
23	TDI	Input	138	24	GND		
25	TDO	Output	120	26	GND		
27	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	128	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{RESETP}}$	Output	193	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

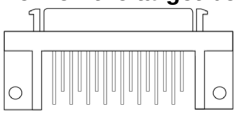
Target connection reference diagram



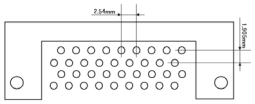
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

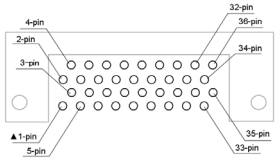
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Mictor connector

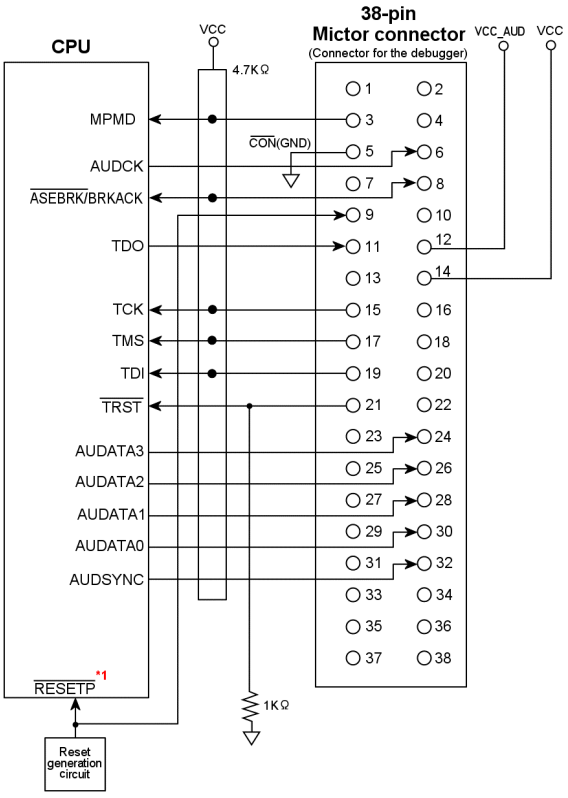
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KB-A	Pin No.	Signal	Input/ Output*1	CPU Pin No. PLQP0208KB-A
1	N.C.			2	N.C.		
3	GND (MPMD) *2	(Input)	(127)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output	124
7	N.C.			8	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	128
9	$\overline{\text{RESETP}}$	Output	193	10	N.C.		
11	TDO	Output	120	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	139	16	N.C.		
17	TMS	Input	137	18	N.C.		
19	TDI	Input	138	20	N.C.		
21	$\overline{\text{TRST}}$	Input	136	22	N.C.		
23	N.C.			24	AUDATA3	Output	130
25	N.C.			26	AUDATA2	Output	131
27	N.C.			28	AUDATA1	Output	133
29	N.C.			30	AUDATA0	Output	135
31	N.C.			32	AUDSYNC	Output	129
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 3 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

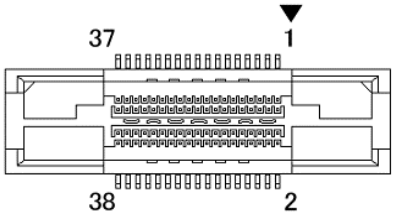
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{RESETP}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{RESETP}}$ pin of CPU.

Document change history (SH7730)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7763

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

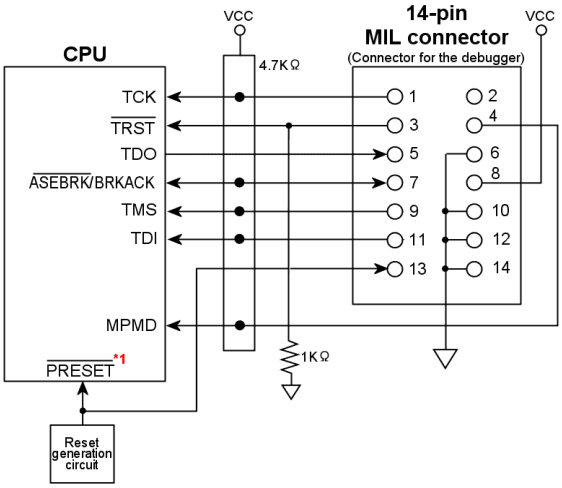
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449
1	TCK	Input	AE19	2	N.C.		
3	$\overline{\text{TRST}}$	Input	AC19	4	GND (MPMD) *2	(Input)	(AB16)
5	TDO	Output	AB20	6	GND		
7	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	AD19	8	VCC *3	Output	
9	TMS	Input	AC21	10	GND		
11	TDI	Input	AC20	12	GND		
13	$\overline{\text{PRESET}}$	Output	AE16	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

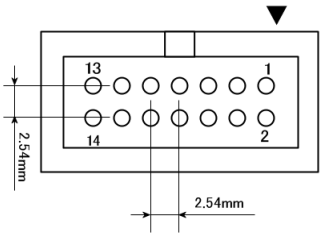
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

MDR connector

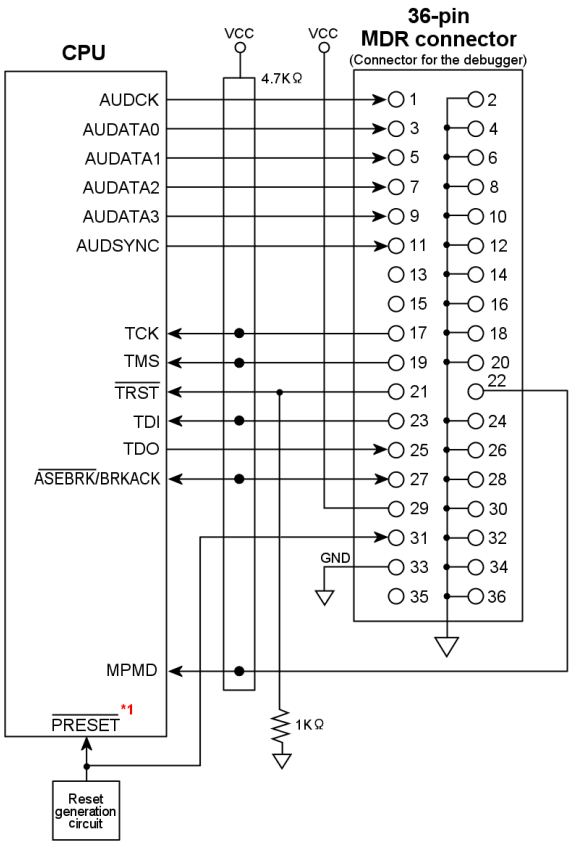
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449	Pin No.	Signal	Input/ Output*1	CPU Pin No. P-FBGA2121-449
1	AUDCK	Output	AE18	2	GND		
3	AUDATA0	Output	AE17	4	GND		
5	AUDATA1	Output	AB18	6	GND		
7	AUDATA2	Output	AC18	8	GND		
9	AUDATA3	Output	AD18	10	GND		
11	AUDSYNC	Output	AD17	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	AE19	18	GND		
19	TMS	Input	AC21	20	GND		
21	$\overline{\text{TRST}}$	Input	AC19	22	GND (MPMD) *2	(Input)	(AB16)
23	TDI	Input	AC20	24	GND		
25	TDO	Output	AB20	26	GND		
27	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	AD19	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{PRESET}}$	Output	AE16	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

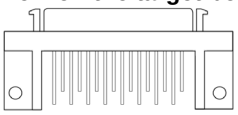
Target connection reference diagram



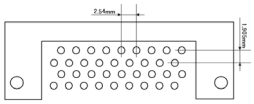
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

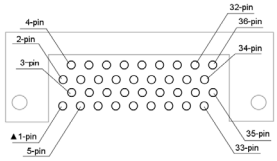
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

Document change history (SH7763)

First Edition	Jun. 30, 2009	Initial edition

SH7764

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design) Mictor connector (38-pin design)

MIL connector

Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-404	Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-404
1	TCK	Input	AB6	2	N.C.		
3	$\overline{\text{TRST}}$	Input	W7	4	GND (MPMD) *2	(Input)	(H4)
5	TDO	Output	W6	6	GND		
7	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	W21	8	VCC *3	Output	
9	TMS	Input	Y6	10	GND		
11	TDI	Input	AA6	12	GND		
13	$\overline{\text{PRESET}}$	Output	Y22	14	GND		

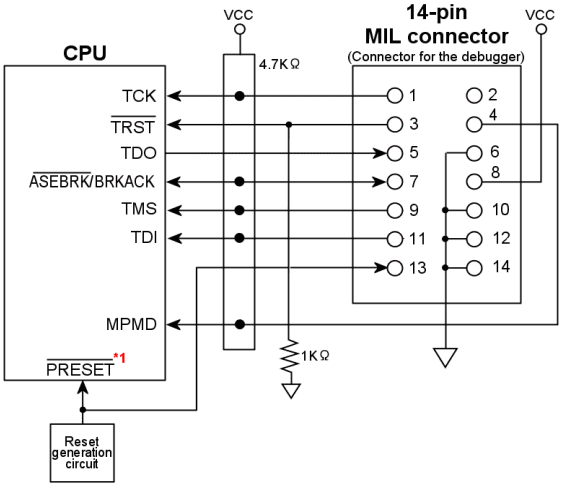
・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.

*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND..

*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

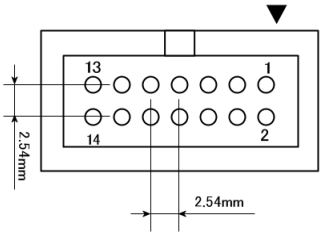
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

MDR connector

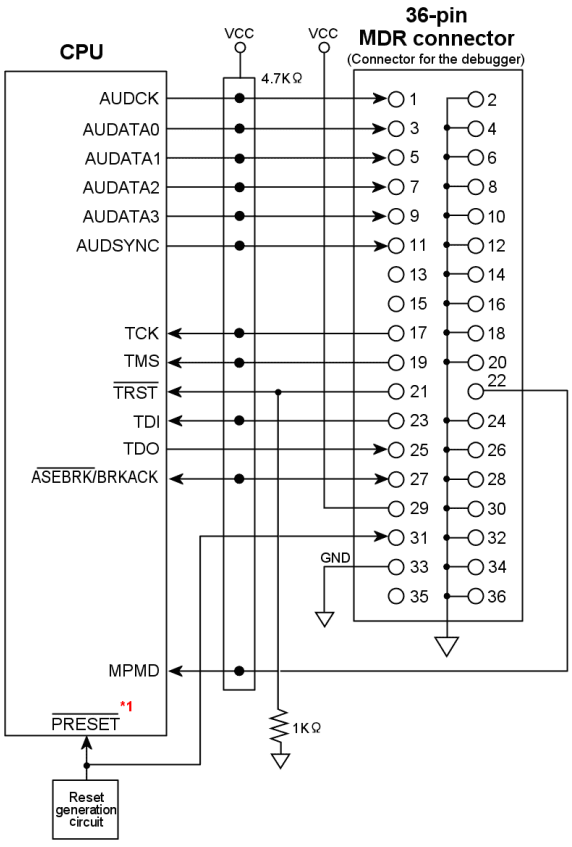
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-404	Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-404
1	AUDCK	Output	W5	2	GND		
3	AUDATA0	Output	Y5	4	GND		
5	AUDATA1	Output	AA5	6	GND		
7	AUDATA2	Output	Y4	8	GND		
9	AUDATA3	Output	AA4	10	GND		
11	AUDSYNC	Output	AB5	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	AB6	18	GND		
19	TMS	Input	Y6	20	GND		
21	$\overline{\text{TRST}}$	Input	W7	22	GND (MPMD) *2	(Input)	(H4)
23	TDI	Input	AA6	24	GND		
25	TDO	Output	W6	26	GND		
27	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	W21	28	GND		
29	VCC *3	Output		30	GND		
31	$\overline{\text{PRESET}}$	Output	Y22	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

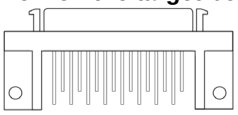
Target connection reference diagram



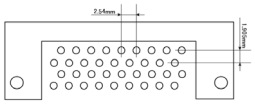
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

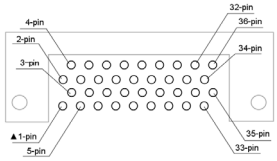
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

Mictor connector

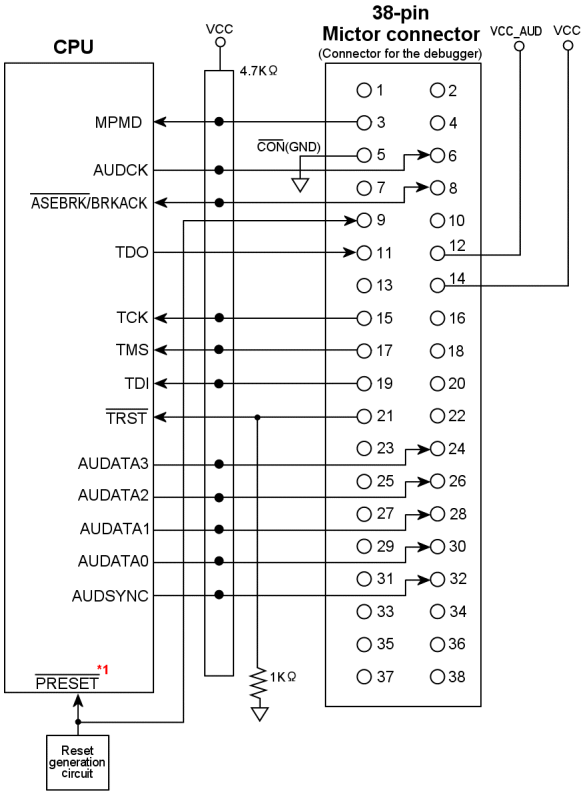
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-404	Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-404
1	N.C.			2	N.C.		
3	GND (MPMD) *2	(Input)	(H4)	4	N.C.		
5	GND ($\overline{\text{CON}}$) *5	(Output)		6	AUDCK	Output	W5
7	N.C.			8	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	W21
9	$\overline{\text{PRESET}}$	Output	Y22	10	N.C.		
11	TDO	Output	W6	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	AB6	16	N.C.		
17	TMS	Input	Y6	18	N.C.		
19	TDI	Input	AA6	20	N.C.		
21	$\overline{\text{TRST}}$	Input	W7	22	N.C.		
23	N.C.			24	AUDATA3	Output	AA4
25	N.C.			26	AUDATA2	Output	Y4
27	N.C.			28	AUDATA1	Output	AA5
29	N.C.			30	AUDATA0	Output	Y5
31	N.C.			32	AUDSYNC	Output	AB5
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 3 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to I/O power of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O power of CPU.
*5: By detection of GND on the target system side, whether the target system is connected or not is determined.

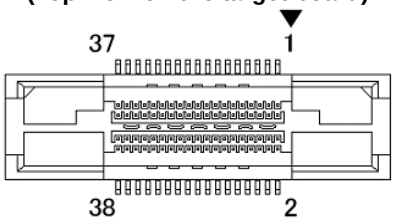
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

Document change history (SH7764)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	Made provision of support for Mictor connector.

SH7770

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

For details of connector interface, please contact us.

Document change history (SH7770)

First Edition	Jun. 30, 2009	Initial edition

SH7774

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

For details of connector interface, please contact us.

Document change history (SH7774)

First Edition	Jun. 30, 2009	Initial edition

SH7780

Applicable products	PALMiCE3-SH / PALMiCE2-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

MIL connector

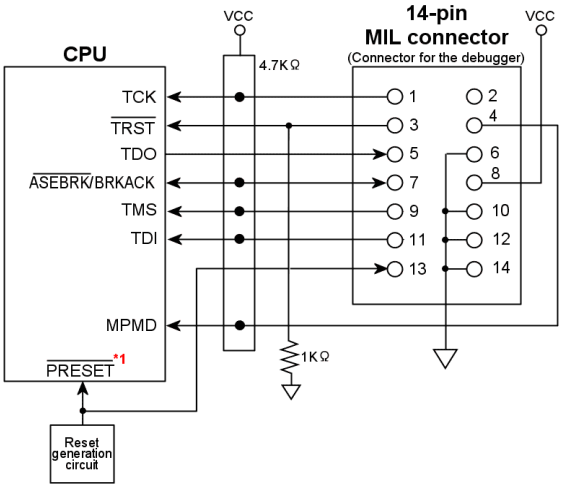
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-449	Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-449
1	TCK	Input	C16	2	N.C.		
3	$\overline{\text{TRST}}$	Input	D17	4	GND (MPMD) *2	(Input)	(AC25)
5	TDO	Output	B17	6	GND		
7	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	C17	8	VCC *3	Output	
9	TMS	Input	D16	10	GND		
11	TDI	Input	A17	12	GND		
13	$\overline{\text{PRESET}}$	Output	A12	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND..
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

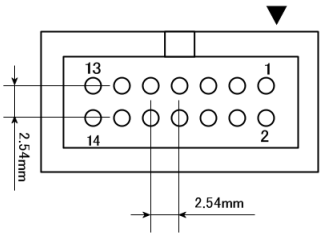
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentatio by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

MDR connector

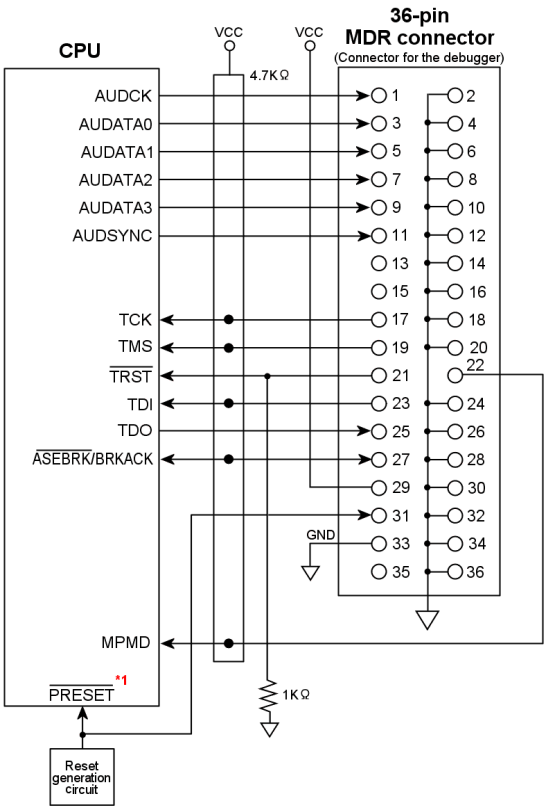
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 BGA-449	Pin No.	Signal	Input/ Output*1	CPU Pin No.*2 BGA-449
1	AUDCK	Output	B18/B13	2	GND		
3	AUDATA0	Output	B19/C14	4	GND		
5	AUDATA1	Output	A19/A15	6	GND		
7	AUDATA2	Output	D18/A16	8	GND		
9	AUDATA3	Output	C18/B16	10	GND		
11	AUDSYNC	Output	A18/C13	12	GND		
13	N.C.			14	GND		
15	N.C.			16	GND		
17	TCK	Input	C16	18	GND		
19	TMS	Input	D16	20	GND		
21	$\overline{\text{TRST}}$	Input	D17	22	GND (MPMD) *3	(Input)	(AC25)
23	TDI	Input	A17	24	GND		
25	TDO	Output	B17	26	GND		
27	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	C17	28	GND		
29	VCC *4	Output		30	GND		
31	$\overline{\text{PRESET}}$	Output	A12	32	GND		
33	GND			34	GND		
35	N.C.			36	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: 2 routings of AUD ports are available. Choose either of them.
*3: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 22 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 22 of the connector for debugger, but connect Pin No. 22 of connector for the debugger to GND.
*4: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

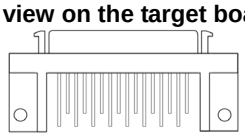
Target connection reference diagram



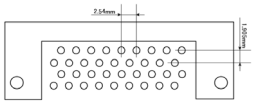
MDR connector specifications

Recommended connector
Manufacturer 3M
Model 10236-52A2JL

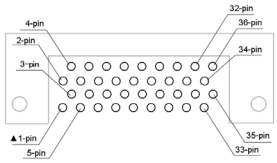
(Top view on the target board)



(Side view on the target board)



(Pin Configuration)



(For detailed dimensions of the connector,
refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 31 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

Document change history (SH7780)

First Edition	Feb. 12, 2008	Initial edition
Second Edition	Jun. 30, 2009	・ **Added PALMiCE3-SH to Applicable products following the release of PALMiCE3-SH.** ・ **Changed the descriptions of AUDSYNC signal regarding the following CPUs.** They had been written in negative logic, however, the descriptions were changed to positive logic so that they conform to the descriptions in the hardware manual published by Renesas Technology Corp..

SH7781

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) MDR connector (36-pin design)

For details of connector interface, please contact us.

Document change history (SH7781)

First Edition	Jun. 30, 2009	Initial edition

SH7785

Applicable product	PALMiCE3-SH
Applicable connectors (Connectors for debugger)	MIL connector (14-pin design) Mictor connector (38-pin design)

MIL connector

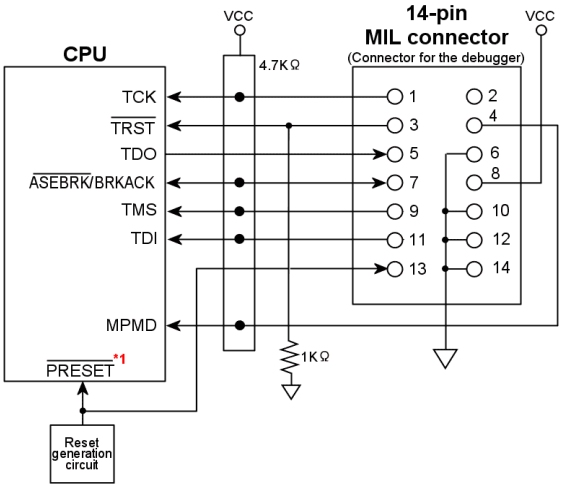
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-436	Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-436
1	TCK	Input	A14	2	N.C.		
3	$\overline{\text{TRST}}$	Input	C15	4	GND (MPMD) *2	(Input)	(C18)
5	TDO	Output	E13	6	GND		
7	$\overline{\text{ASEBRK}}$/BRKACK	Input/Output	C14	8	VCC *3	Output	
9	TMS	Input	E15	10	GND		
11	TDI	Input	B14	12	GND		
13	$\overline{\text{PRESET}}$	Output	N1	14	GND		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 4 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 4 of the connector for debugger, but connect Pin No. 4 of connector for the debugger to GND..
*3: For VCC, connect I/O power of CPU. Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.

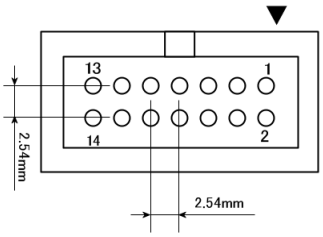
Target connection reference diagram



MIL connector specifications

Recommended connector
Manufacturer Omron Corporation
Model XG4C-1431

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentatio by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: $\overline{\text{PRESET}}$, which is connected to Pin No. 13 of the connector for debugger, is the signal that debugger uses for monitoring the state of $\overline{\text{PRESET}}$ pin of CPU.

Mictor connector

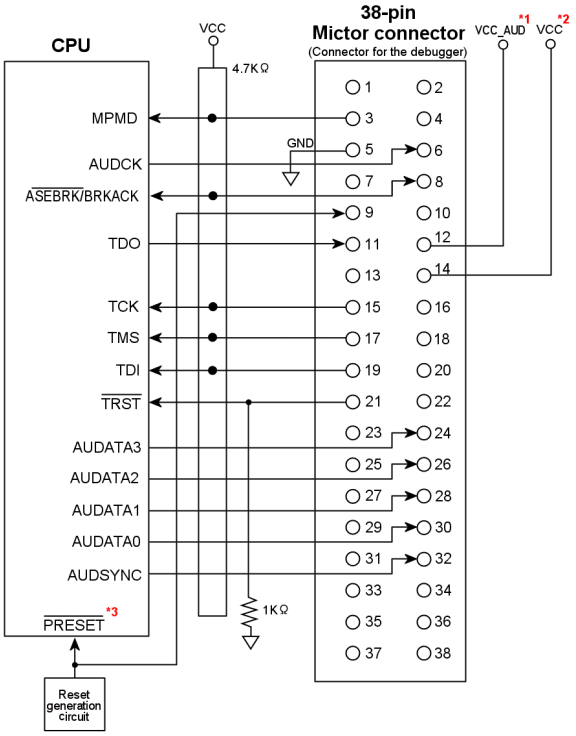
Signals

Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-436	Pin No.	Signal	Input/ Output*1	CPU Pin No. BGA-436
1	N.C.			2	N.C.		
3	GND (MPMD) *2	(Input)	(C18)	4	N.C.		
5	GND			6	AUDCK	Output	A13
7	N.C.			8	ASEBRK/BRKACK	Input/Output	C14
9	PRESET	Output	N1	10	N.C.		
11	TDO	Output	E13	12	VCC_AUD *3	Output	
13	N.C.			14	VCC *4	Output	
15	TCK	Input	A14	16	N.C.		
17	TMS	Input	E15	18	N.C.		
19	TDI	Input	B14	20	N.C.		
21	TRST	Input	C15	22	N.C.		
23	N.C.			24	AUDATA3	Output	C13
25	N.C.			26	AUDATA2	Output	B12
27	N.C.			28	AUDATA1	Output	D12
29	N.C.			30	AUDATA0	Output	C12
31	N.C.			32	AUDSYNC	Output	A12
33	N.C.			34	N.C.		
35	N.C.			36	N.C.		
37	N.C.			38	N.C.		

・ For the pin where stated as N.C. in the table, leave the signal unconnected.

*1: Input/output is based on the target system.
*2: To debug, MPMD pin needs to be brought to Low state.
Shown in the target connection reference diagram is the circuit that brings MPMD pin to Low state when you connect MPMD signal to the connector for debugger. If you do not connect MPMD signal to Pin No. 3 of the connector for debugger, the circuit that sets MPMD pin by switch circuit will do. However, in such case, do not connect MPMD pin to Pin No. 3 of the connector for debugger, but connect Pin No. 3 of connector for the debugger to GND.
*3: For VCC_AUD, the power same as the voltage level at which AUD signal of CPU works is to be connected. Connect the AUD signal to VDD-DDR(1.8V) of CPU.
*4: For VCC, the power same as the voltage level at which HUDI signal of CPU works is to be connected. Connect the HUDI signal to I/O(3.3V) of CPU.

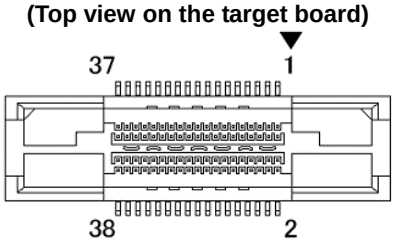
Target connection reference diagram



Mictor connector specifications

Recommended connector
Manufacturer AMP
Model Mictor connector
2-767004-2 / 767054-1 / 767061

(Top view on the target board)



(For detailed dimensions of the connector,
refer to the documentatio by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting. Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

*1: For VCC_AUD, connect VDD-DDR(1.8V) power.
*2: For VCC, connect VDDQ(3.3V). Debugging can be performed even if the signal is N.C., however, by connecting I/O power, leak during the target system power OFF can be prevented.
*3: PRESET, which is connected to Pin No. 9 of the connector for debugger, is the signal that debugger uses for monitoring the state of PRESET pin of CPU.

Document change history (SH7785)

First Edition	Jun. 30, 2009	Initial edition
Second Edition	Jun. 1, 2010	▪ **Mictor connector** Edited the contents of note *3 and *4 of signal table.

PALMiCE3 HUDI140 model

Hardware Manual

(Third Edition)

Go through the required procedures as stated under Foreign Exchange and Foreign Trade Control Law in exporting (including the case where travelers directly carry) this product or providing the software for residents outside Japan.

Table of Contents

Chapter 1 Getting Started

1.1 Introduction

PALMiCE3 HUDI140 model is an on-chip debugger that supports Renesas Electronics-made microcomputers.

Its main features are as follows:

- Provides multi-core support
- No power supply to PALMiCE3 is required (with VBus support)
- Allows downloading to external flash memory and its debugging
- Supports on-chip flash memory
- Versatile
- Supports USB Standard Revision2.0 high-speed and full-speed
- Allows downloading of the latest CSIDE from the Internet
- Designed with palm-sized, light, and compact body

Info.

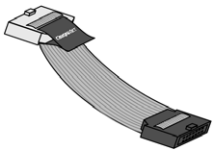
This product supports various series of Renesas Electronics-made CPUs.
Therefore, names of other CPUs besides that of the one you are using are also mentioned in this manual.

1.2 Product Composition Contents

Product composition of PALMiCE3 HUDI140 is as follows.

・PALMiCE3 HUDI140 model ····· x 1

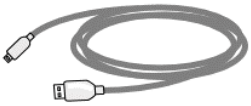
・H-UDI cable (Specifically for PALMiCE3) ····· x 1



・RSTOUT probe (For HUDI140) ····· x 1

・Read before use (Introductory guide) ····· x 1

・USB cable ····· x 1



・Product name sticker ····· x 1

・Software (CD-ROM) *1 ····· x 1

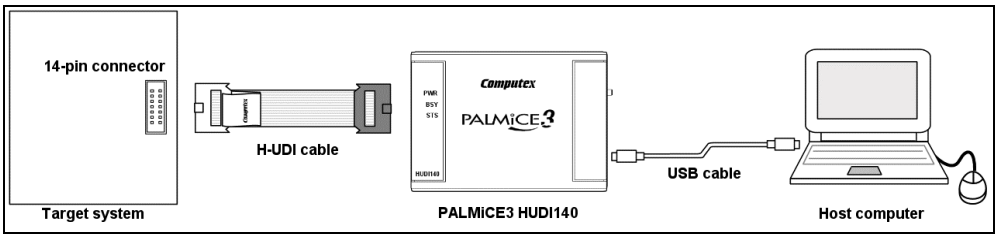
***1 : Its name varies depending on CSIDE, the debugger software you purchased.**

1.3 Connection structure

PALMiCE3 is to be connected to the host computer with the USB cable included with the product. PALMiCE3 is to be connected to the target system with the H-UDI cable included with the product. Also, RSTOUT probe is to be connected as required. For details on RSTOUT probe and the target interface, see the next chapter.

Note

To use PALMiCE3, the interface connector for PALMiCE3 use needs to be mounted on the target system beforehand.



PALMiCE3 HUDI140 model
Connection structure

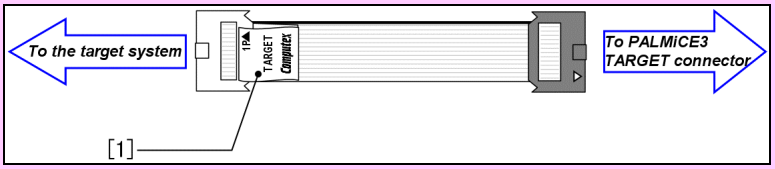
Note

When connecting the hardware,
if you put too much pressure, stress, or strain on the connector, doing so may cause damage.
Be careful not to put too much pressure or try not to strain or put stress on the connector.

Note

About H-UDI cable specifically for PALMiCE3

- Make sure to use PALMiCE3-specific H-UDI cable made by Computex.
- When establishing connections, connect the connector with a tag ([1] in the illustration) to the target system.



Info.

For connection to the target system, optional products such as conversion adapter are available.

Chapter 2
PALMiCE3 HUDI140 Hardware Specifications

2.1 PALMiCE3 HUDI140 model hardware specifications

PALMiCE3 is a purpose-built debugger for utilizing on-chip debugging feature incorporated in Renesas Electronics-made CPU.

PALMiCE3 incorporates on-chip debugging feature to provide the following functionalities.

- Execution and break of the user program
- Break by matching any address and data
- Force break of the user program
- Trace and step executions
- Viewing and editing of memory, register, and I/O

This chapter spells out specifications of PALMiCE3 hardware.

2.2 HUDI140 model specifications

Item		HUDI140 model specifications
Supported CPUs		SH-Mobile SuperH RISC engine family *1 H8SX family H8S family R8J family
Interface *2	Specification of the connector	14-pin MIL connector (Cable length: Approx. 20cm)
	Specification of the connector on the target system side	OMRON-made XG4C-1431 (14-pin)
Target interface voltage		1.65V - 5.5V（Follows target） Note, for 5V-spec CPUs, output level will be min. 4.2V - max. 4.7V.
LED		・PWR ・BSY ・STS
Outside dimensions		95mm(W)×70mm(D)×21mm(H)　(Exclusive of connector)
Operating environment		Operating temperature：5℃ to 40℃ Operating humidity：35% to 85%RH No condensation
USB host interface		USB(Ver2.0)
AC adapter		Not required (Vbus support)
Current consumption		DC5V ±5% Max. approx. 250mA (from USB VBus)
Weight		78g

*1: With the exception of SH7050 series
*2: Support also available for 36-pin MDR connector and 38-pin Mictor connector with optional dedicated adapters.

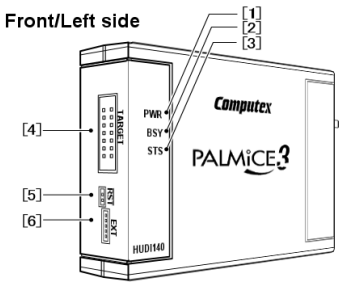
Note

MIL connector:　14-pin connector that supports H-UDI interface
MDR connector: 36-pin connector that supports AUD interface

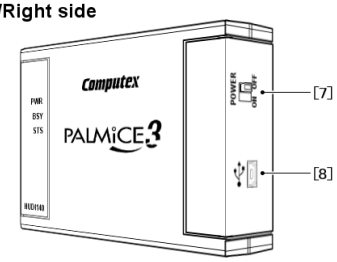
2.3 Name and function of each part

Appearance drawing of PALMiCE3 HUDI140 model is given to the following.

Front/Left side



Front/Right side



[1] PWR LED
Comes on when the power is supplied to PALMiCE3. Power is supplied from the host computer through USB cable.

[2] BSY LED
Flickers during communication between PALMiCE3 and the target CPU.

[3] STS LED
Lit normally during user program execution.
Also, flashes in some cases to notify errors.
For details, refer to the user's manual.

[4] TARGET connector
14-pin connector for connecting PALMiCE3 to the target system.

[5] $\overline{\text{RST}}$
Connect RSTOUT probe to be connected to reset circuit in the target system. (When using PALMiCE3 SuperH)

[6] EXT
Currently not used.

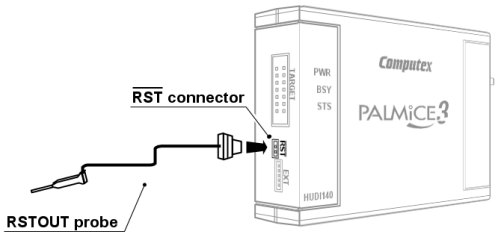
[7] Power switch
Turns ON/OFF the PALMiCE3's power. Power input state can be checked with [1] POWER LED.

[8] USB connector
Connect USB cable. (mini-B type connector)

2.3.1 RSTOUT probe

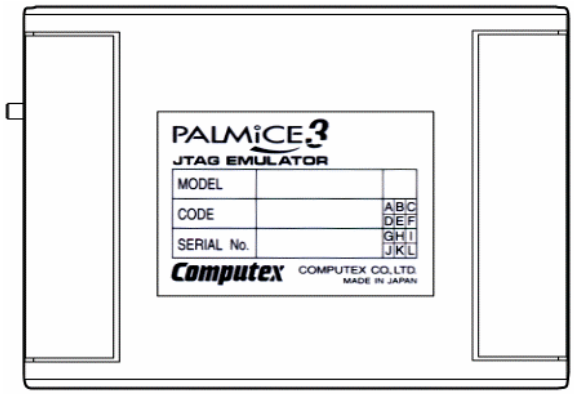
■ When using PALMiCE3 SuperH

RSTOUT probe is to be used when you are using PALMiCE3 HUDI140 model and outputting reset signal to the target system.



2.3.2 Hardware revision

The sticker with PALMiCE3 information is placed at the back of PALMiCE3 main unit.



Back side of PALMiCE3 main unit

How revision sticker reads

Read the number given on the upper side and the last alphabet shaded with black.

Example 1): Hardware revision 1-B

1		
A	**B**	C
D	E	F
G	H	I
J	K	L

In Example 1), PALMiCE3 hardware revision reads as 1-B.

Example 2): Hardware revision 2-0

2		
A	B	C
D	E	F
G	H	I
J	K	L

In Example 2), where alphabets are not shaded, PALMiCE3 hardware revision reads as 2-0.

Chapter 3 Target Interface Specifications

3.1 Introduction

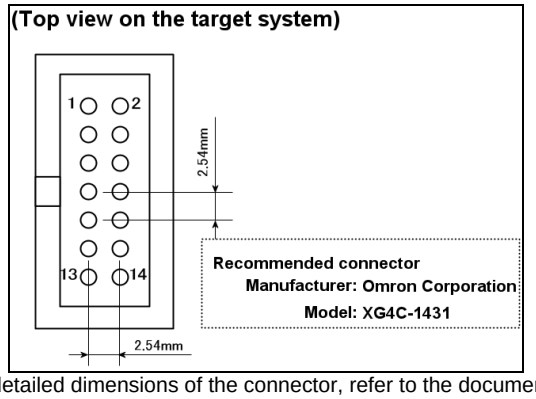
This Chapter spells out H-UDI interface specifications for connecting PALMiCE3 HUDI140 to the target system.

3.2 H-UDI interface

The interface for connecting PALMiCE3 HUDI140 to the target system is described.
Target interface varies from CPU to CPU.

3.2.1 Shape of the connector for debugger

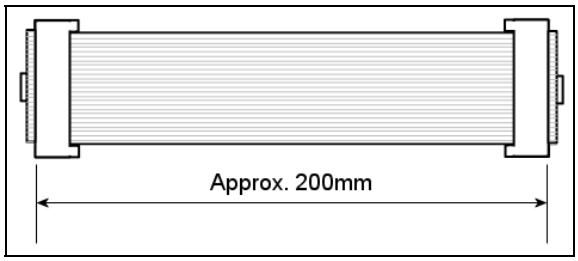
The shape of connector(14-pin MIL connector) for debugger to be mounted on the target system side is as follows.



(For detailed dimensions of the connector, refer to the documentations provided by manufacturers.)

3.2.2 Dimensions of H-UDI cable

The dimensions of H-UDI cable for connecting PALMiCE3 HUDI140 to the target system are as follows.

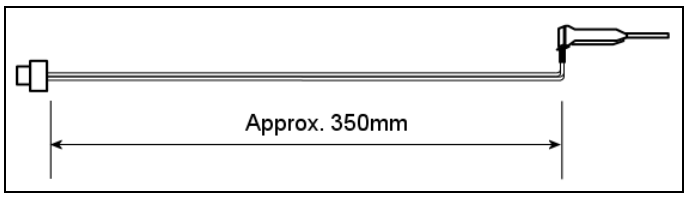


(For detailed dimensions of the connector, refer to the documentations provided by manufacturers.)

3.2.3 Dimensions of RSTOUT probe

■ When using PALMiCE3 SuperH

The dimensions of RSTOUT probe are as follows.



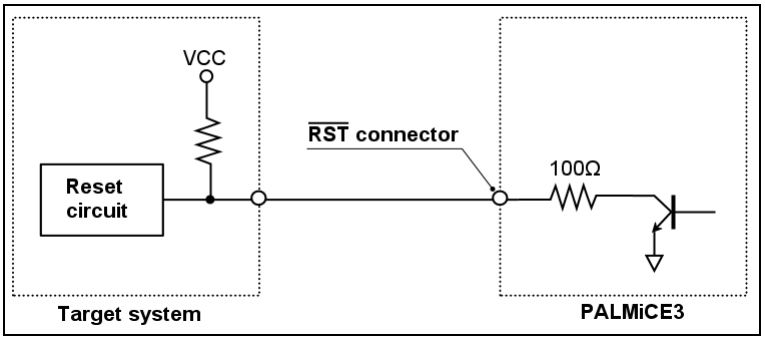
3.2.4 Specifications of H-UDI interface signals

Input voltage level	VIL	Target voltage ÷ 2 – 0.35
	VIH	Target voltage ÷ 2 + 0.35
Output voltage level	VOL	Under 0.2V
	VOH	Follows the target voltage (Note, for 5V-spec CPUs, output level will be min. 4.2V - max. 4.7V.)

3.2.5 RSTOUT signal

■ When using PALMiCE3 SuperH

/RSTOUT signal is a signal for requesting reset from PALMiCE3 to the target system. The signal will be output by open-collector circuit if from PALMiCE3.
Connect this signal to the reset circuit of the whole target system inclusive of CPU and peripherals. It is required for synchronization at CSIDE startup.
If connection can not be established, you can still press reset switch button on the target system or use power-on-reset.



3.2.6 The target interface on PALMiCE3 side

The target interface on PALMiCE3 side is described.

No.	Signal	Remarks	No.	Signal	Remarks
1	TCK	33Ω Series	2	GND	
3	$\overline{\text{TRST}}$	33Ω Series	4	GND ($\overline{\text{ASEMD}}$)	
5	TDO	33Ω Series 10KΩ Pull-up*1	6	GND	
7	$\overline{\text{ASEBRKAK}}$	100Ω Series 10KΩ Pull-up*1	8	VCC	
9	TMS	33Ω Series	10	GND	
11	TDI	33Ω Series	12	GND	
13	$\overline{\text{RESET}}$	100Ω Series 100KΩ Pull-down	14	GND	

*1: Potential has been pulled up to the same level as target VCC reference voltage.

Note

Each name of the signal varies depending on the CPU you use.

Note

Besides this manual, also, consult "Technical Information on PALMiCE3" up on our website (http://www.computex.co.jp/eg/)

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PALMiCE3 HUDI140 model Hardware Manual
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CM845(C)1101

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PALMiCE3 AUD360 model

Hardware Manual

(Fourth Edition)

Go through the required procedures as stated under Foreign Exchange and Foreign Trade Control Law in exporting (including the case where travelers directly carry) this product or providing the software for residents outside Japan.

Table of Contents

Chapter 1 Getting Started

1.1 Introduction

PALMiCE3 AUD360 model is an on-chip debugger that supports microcomputers made by Renesas Electronics.

Its main features are as follows:

- Supports AUD tracing functionality
  ・Module measurement feature
  ・Function transition display feature
  ・Trace-back feature (Optional)
- Provides multi-core support
- No power supply to PALMiCE3 is required (with VBus support)
- Allows downloading to external flash memory and its debugging
- Supports on-chip flash memory (SH-2 embedded with flash memory)
- Versatile
- Supports USB Standard Revision2.0 high-speed and full-speed
- Allows downloading of the latest CSIDE from the Internet
- Designed with palm-sized, light, and compact body

Info.

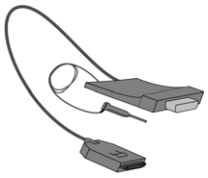
This product supports various series of CPUs made by Renesas Electronics.
Therefore, names of other CPUs besides that of the one you are using are also mentioned in this manual.

1.2 Product Composition Contents

Product composition of PALMiCE3 AUD360 is as follows.

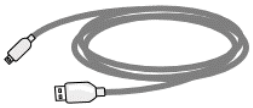
・PALMiCE3 AUD360 model ····· x 1

・AUD probe (Specifically for PALMiCE3) ····· x 1



・Read before use (Introductory guide) ····· x 1

・USB cable ····· x 1



・Product name sticker ····· x 1

・Software (CD-ROM) *1 ····· x 1

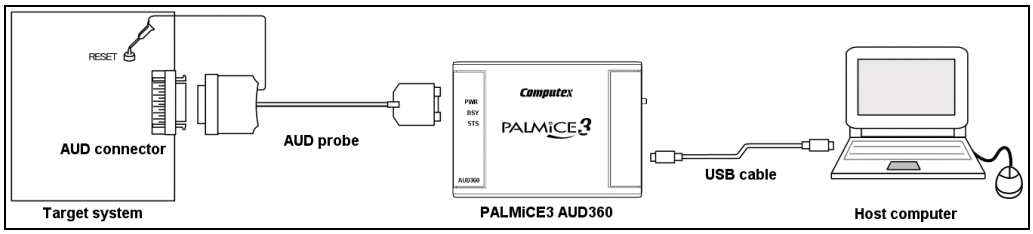
***1 : Its name varies depending on CSIDE, the debugger software you purchased.**

1.3 Connection structure

PALMiCE3 is to be connected to the host computer with the USB cable included with the product. PALMiCE3 is to be connected to the target system with the AUD probe included with the product. Also, RSTOUT probe is to be connected as required. For details on RSTOUT probe and the target interface, see the next chapter.

Note

To use PALMiCE3, the interface connector for PALMiCE3 use needs to be mounted on the target system beforehand.



PALMiCE3 AUD360 model
Connection structure

Note

When connecting the hardware,
if you put too much pressure, stress, or strain on the connector, doing so may cause damage.
Be careful not to put too much pressure or try not to strain or put stress on the connector.

Info.

For connection to the target system, optional products such as conversion adapter and ICE-ADP are available.

Chapter 2
PALMiCE3 AUD360 Hardware Specifications

2.1 PALMiCE3 AUD360 model hardware specifications

PALMiCE3 is a purpose-built debugger for utilizing on-chip debugging feature incorporated in the CPUs made by Renesas Electronics.

PALMiCE3 incorporates on-chip debugging feature to provide the following functionalities.

- Execution and break of the user program
- Break by matching any address and data
- Force break of the user program
- Trace and step executions
- Viewing and editing of memory, register, and I/O
- Large-capacity branch tracing with time stamp

This chapter spells out specifications of PALMiCE3 hardware.

2.2 AUD360 model specifications

Item		AUD360 model specifications
Supported CPUs		SH-Mobile SuperH family
Branch tracing memory for AUD		Max. 512K frame
Time stamp (Branch tracing memory)		32-bit (Clock 1us or 50nS to choose from)
Interface *1	Specification of the connector	36-pin MDR connector (Cable length: Approx. 33cm)
	Specification of the connector on the target system side	3M-made 10236-52A2JL
Target interface voltage		Output*2 :1.2V - 3.6V (Follows target) or fixed to 3.3V Input : 5V-torelant
LED		・PWR ・BSY ・STS
Outside dimensions		95mm(W)X70mm(D)X21mm(H) (Exclusive of connector)
Operating environment		Operating temperature: 5℃ to 40℃ Operating humidity: 35% to 85%RH No condensation
USB host interface		USB(Ver2.0)
AC adapter		Not required (Vbus support)
Current consumption		DC5V ±5% Max. approx. 350mA (from USB VBus)
Weight		78g

*1 : Support also available for 14-pin MIL connector and 38-pin Mictor connector with optional dedicated adapters.
*2 : In the case of $\overline{\text{TRST}}$ signal, it will be 1.8V - 5.5V (Follows target)

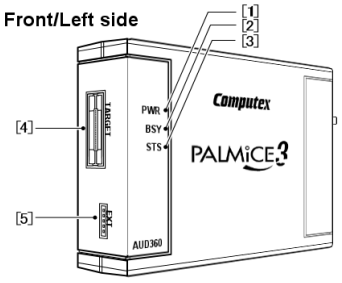
Note

MDR connector: 36-pin connector that supports AUD interface
MIL connector: 14-pin connector that supports H-UDI interface

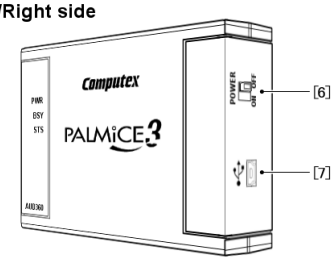
2.3 Name and function of each part

Appearance drawing of PALMiCE3 AUD360 model is given to the following.

Front/Left side



Front/Right side



[1] PWR LED
Comes on when the power is supplied to PALMiCE3. Power is supplied from the host computer through USB cable.

[2] BSY LED
Flickers during communication between PALMiCE3 and the target CPU.

[3] STS LED
Lit normally during user program execution.
Also, flashes in some cases to notify errors.
For details, refer to the user's manual.

[4] TARGET connector
36-pin connector for connecting PALMiCE3 to the target system.

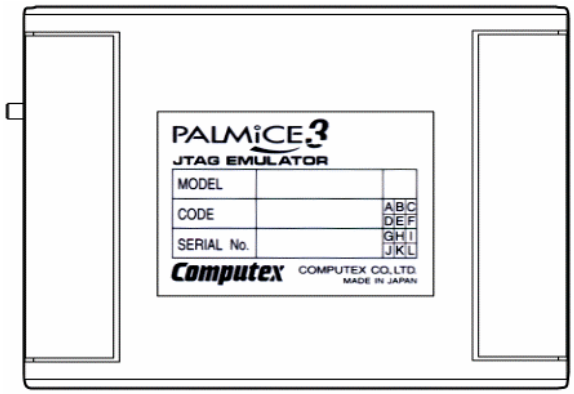
[5] EXT
Currently not used.

[6] Power switch
Turns ON/OFF the PALMiCE3's power. Power input state can be checked with [1] POWER LED.

[7] USB connector
Connect USB cable. (mini-B type connector)

2.3.1 Hardware revision

The sticker with PALMiCE3 information is placed at the back of PALMiCE3 main unit.



Back side of PALMiCE3 main unit

How revision sticker reads

Read the number given on the upper side and the last alphabet shaded with black.

Example 1): Hardware revision 1-B

1		
A	**B**	C
D	E	F
G	H	I
J	K	L

In Example 1), PALMiCE3 hardware revision reads as 1-B.

Example 2): Hardware revision 2-0

2		
A	B	C
D	E	F
G	H	I
J	K	L

In Example 2), where alphabets are not shaded, PALMiCE3 hardware revision reads as 2-0.

Chapter 3 Target Interface Specifications

3.1 Introduction

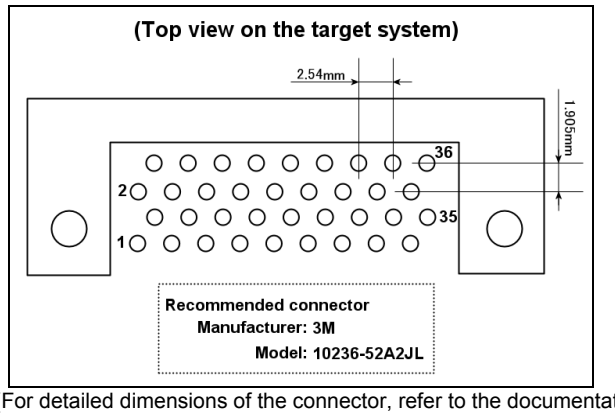
This Chapter spells out AUD interface specifications for connecting PALMiCE3 AUD360 to the target system.

3.2 AUD interface

The interface for connecting PALMiCE3 AUD360 to the target system is described.
AUD360 supports AUD interface. Target interface varies from CPU to CPU.

3.2.1 Shape of the connector for debugger

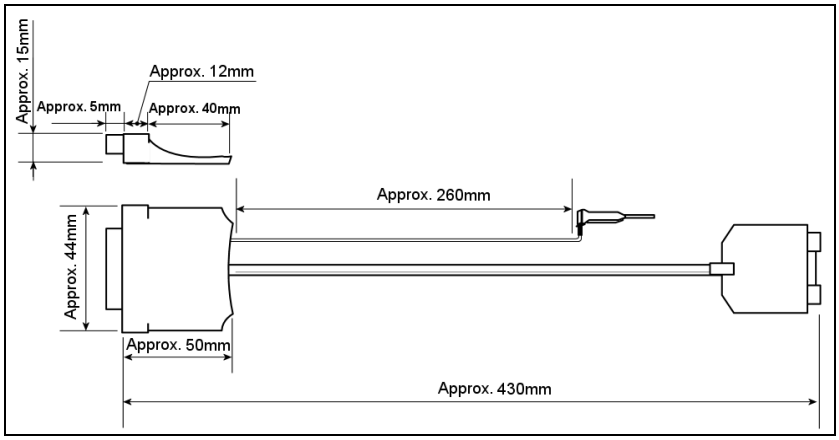
The shape of connector (36-pin MDR connector) for debugger to be mounted on the target system side is as follows.



(For detailed dimensions of the connector, refer to the documentations provided by manufacturers.)

3.2.2 Dimensions of AUD probe

The dimensions of AUD probe for connecting PALMiCE3 AUD360 to the target system are as follows.



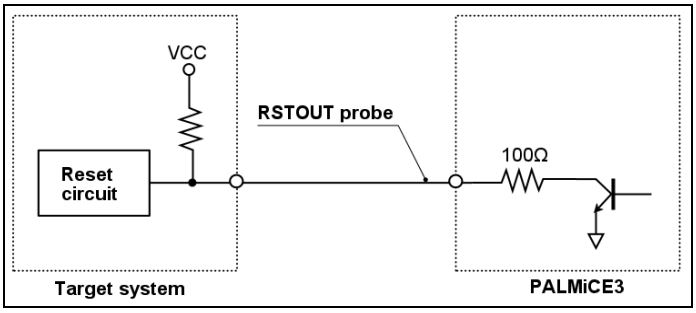
3.2.3 Specifications of AUD interface signals

Input voltage level	VIL	Target voltage ÷ 2 – 0.35
	VIH	Target voltage ÷ 2 + 0.35
Output voltage level	VOL	Under 0.2V
	VOH	Follows the target voltage (1.2V - 3.6V) *1

*1 : In the case of $\overline{\text{TRST}}$ signal, it will be 1.8V - 5.5V (Follows target)

3.2.4 RSTOUT signal

/RSTOUT signal is a signal for requesting reset from PALMiCE3 to the target system. The signal will be output by open-collector circuit if from PALMiCE3.
Connect this signal to the reset circuit of the whole target system inclusive of CPU and peripherals. It is required for synchronization at CSIDE startup.
If connection can not be established, you can still press reset switch button on the target system or use power-on-reset.



3.2.5 The target interface on PALMiCE3 side

The target interface on PALMiCE3 side is described.

No.	Signal	Remarks	No.	Signal	Remarks
1	AUDCK2	33Ω Series	2	GND	
3	AUDATA0	33Ω Series	4	GND	
5	AUDATA1	33Ω Series	6	GND	
7	AUDATA2	33Ω Series	8	GND	
9	AUDATA3	33Ω Series	10	GND	
11	$\overline{\text{AUDSYNC}}$	33Ω Series	12	GND	
13	$\overline{\text{AUDRST}}$	33Ω Series	14	GND	
15	AUDMD	33Ω Series	16	GND	
17	TCK	33Ω Series	18	GND	
19	TMS	33Ω Series	20	GND	
21	$\overline{\text{TRST}}$	33Ω Series	22	GND ($\overline{\text{ASEMD}}$)	
23	TDI	33Ω Series	24	GND	
25	TDO	33Ω Series 10KΩ Pull-up*1	26	GND	
27	$\overline{\text{ASEBRK}}$	33Ω Series 10KΩ Pull-up*1	28	GND	
29	VCC	100Ω Series	30	GND	
31	$\overline{\text{RESET}}$	100Ω Series 100KΩ Pull-down	32	GND	
33	$\overline{\text{SENSE}}$	100Ω Series	34	GND	
35	AUDCK1	33Ω Series	36	GND	

*1 : Potential has been pulled up to the same level as target VCC reference voltage.

Note

Each name of the signal varies depending on the CPU you use.

Note

Besides this manual, also, consult "Technical Information on PALMiCE3" up on our website (http://www.computex.co.jp/eg/)

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