On-board Flash Programmer
FP-40 Technical Information

Eighth Edition (Jan. 22, 2025)

Table of Contents

Document change history

First Edition	Jul. 01, 2023	Initial edition
Second Edition	Aug. 31, 2023	Added description of drive specs to External I/O
Third Edition	Feb. 05, 2024	Added description of the TLCS-870/C1 series to UART. Regarding the reference circuit diagram in ③, pins 11 and 13 have been changed to N.C.
Forth Edition	Feb. 29, 2024	Corrected a typographical error in the description of the TLCS-870/C1 series of UARTs.
Fifth Edition	Jun. 28, 2024	Changed the product name of the optional product "SWJ-PRB-MIL20-20HP" to "SWJ-PRB-MIL20-20HP-P5V". Added explanation for pins 11 and 13 in the reference circuit diagrams ③ and ④.
Sixth Edition	Aug. 02, 2024	Corrected a typographical error in the description of the UART signals.
Seventh Edition	Dec. 02, 2024	Rearrangement.
Eighth Edition	Jan. 22, 2025	Corrected a typographical error in the description of the signal table.

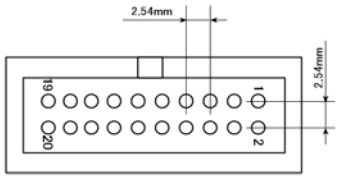
arm Cortex series (JTAG/SWD)

This section describes the specifications for connecting a CPU with a core such as Cortex-M7 or Cortex-A9 to FP-40. The Cortex core has a dedicated debugging function called DAP. FP-40 uses this debugging function to control the CPU to write to flash memory. SWD or JTAG is used for communication with the DAP. SWD is an ARM proprietary specification that extends JTAG and uses only the TMS and TCK signals of JTAG. Also, when using JTAG, the TRST signal may be required, or special processing may be required to use debugging functions. Please be sure to check the CPU manual before use. This technical document describes general interface specifications.

Supported connectors

(For detailed dimensions of the connectors, refer to the documentations by respective manufacturers of the connectors.)

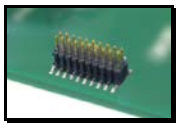
20-pin 2.54mm-pitch connector

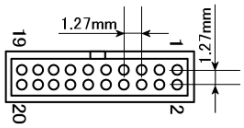


(Top view on the target board)

Recommended connector
Manufacturer: OMRON Corporation
Model : XG4C-2031

20-pin 1.27mm-pitch connector*1

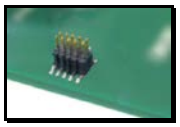


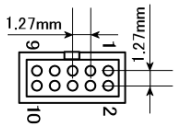


(Top view on the target board)

Recommended connector
Manufacturer: Samtec, Inc.
Model : FTSH-110-01-L-DV-K

10-pin 1.27mm-pitch connector*2





(Top view on the target board)

Recommended connector
Manufacturer: Samtec, Inc.
Model : FTSH-105-01-L-DV-K

*1: **Requires a target probe "SWJ-PRB-MIL20-20HP-P5V" (Optional product).**
*2: **Requires a target probe "SWJ-PRB-MIL20-10HP" (Optional product).**

* Before connecting, please refer the pin configuration diagram and make sure that the connector is in the right direction and the signals and pin numbers match. In addition to our own specifications, each company may have extended their own specifications, so be sure to check the signal names as well. The signal may be shorted and cause a malfunction.

Applicable products

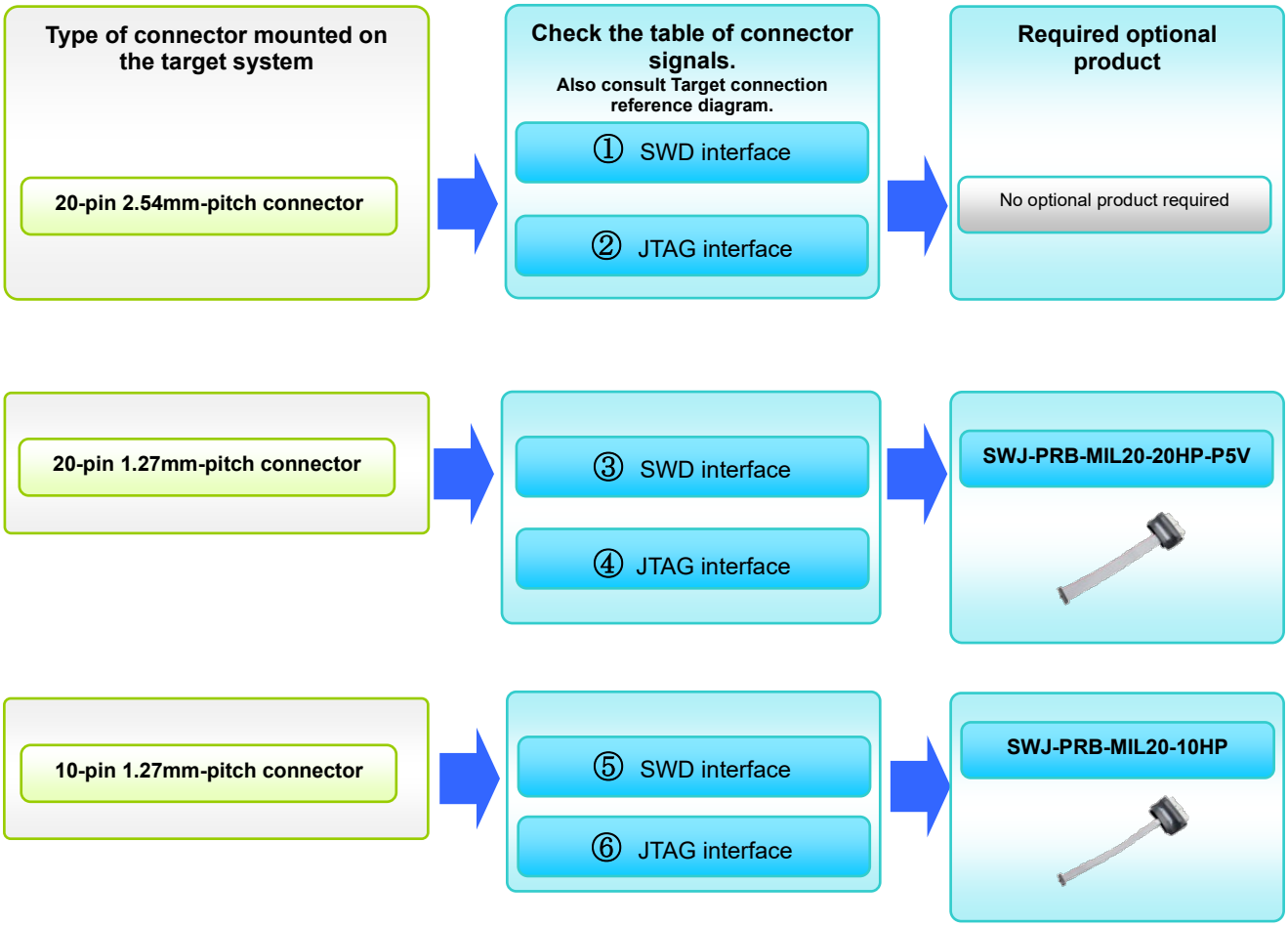
This manual is applicable for the following products:

- On-board Flash Programmer FP-40

* FP-40 is the upgraded model of FP-10/FP-10(model PS). The interface specifications are compatible with those of FP-10/FP-10(model PS), so existing users can replace their FP-10/FP-10(model PS) with FP-40 without modification.

FP-40 usage environment check chart

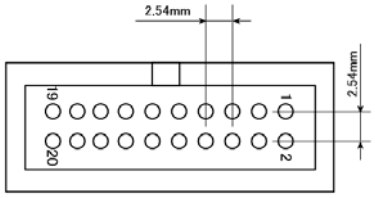
The following chart table summarizes the conditions required to connect a CPU employing a Cortex core to FP-40.
With reference to the chart below, check to see if the current environment is suitable for FP-40 use.



* If you are using a CPU that requires $\overline{\text{TRST}}$, ⑤ and ⑥ cannot be used; $\overline{\text{TRST}}$ is not provided for SWJ-PRB-MIL20-10HP.

20-pin 2.54mm-pitch connector

Target connector specifications



(Top view on the target board)

Recommended connector
Manufacturer: OMRON Corporation
Model: XG4C-2031

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please refer the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

① SWD interface

The SWD interface signal table when connected with a 20-pin 2.54mm pitch connector is shown below.
In addition to the standard SWD signals, a power supply function and external input/output functions are supported via Connectionthe FP-40's unique signals.

Signal description

Pin No.	SWD I/F		FP-40		FP-40 unique Specifications	Connection
	Signal	Input/ Output*1	Signal	Input/ Output*1		
1	VTref	Output	VTref	Output	-	Connect the I/O power supply of the CPU to be connected.
2	TVDD	Output	**X3.3V (N.C.)**	**Input**	**Yes**	TVDD signal is not used in FP-40. X3.3V is a FP-40 unique signal and can be used as 3.3V power supply function. Please note that this signal should not be used if X5V(Pin 20) is used as the power supply. When not used, leave as NC.
3	N.C.	-	**EX_BSY (N.C.)**	**Input**	**Yes**	EX_BSY is a FP-40 unique signal and outputs the operation status from FP-40. When not used, leave as NC.
4	GND	-	GND	-	-	
5	N.C.	-	**EX_NG (N.C.)**	**Input**	**Yes**	EX_NG is an FP-40 original signal and outputs the operation status from FP-40. When not used, leave as NC.
6	GND	-	GND	-	-	
7	SWDIO	Input/Output	SWDIO	Input/Output	-	
8	GND	-	GND	-	-	
9	SWCLK	Input	SWCLK	Input	-	
10	GND	-	GND	-	-	
11	N.C.	-	**EX_STARTn (N.C.)**	**Output**	**Yes**	EX_STARTn is a FP-40 unique signal and can be used as a write start request signal to FP-40. When not used, leave as NC.
12	GND	-	GND	-	-	
13	SWO	Output	N.C.	-	Yes	NC as this signal is not used.
14	GND	-	GND	-	-	
15	SRSTn	Input	SRSTn	Input	-	Connect the reset signal to the connected CPU with a wired OR circuit or an OR circuit. The SRSTn signal is an open collector output.
16	GND	-	**EX33_BSY (N.C.)**	**Input**	**Yes**	EX33_BSY is an FP-40 original signal and outputs the operation status from FP-40. When not used, leave as NC.
17	N.C.	-	**EX_OK (N.C.)**	**Input**	**Yes**	EX_OK is an FP-40 original signal and outputs the operation status from FP-40. When not used, leave as NC.
18	GND	-	**EX33_OK (N.C.)**	**Input**	**Yes**	EX33_OK is an FP-40 original signal and outputs the operation status from FP-40. When not used, leave as NC.
19	N.C.	-	**EX33_STARTn (N.C.)**	**Output**	**Yes**	EX33_STARTn is an FP-40 original signal and can be used as a write start request signal to FP-40. When not used, leave as NC.
20	GND	-	**X5V (N.C.)**	**Input**	**Yes**	X5V is FP-40's unique signal and can be used as 5V power supply function. Cannot be used with 2-pin 3.3V power supply. If not used, leave as NC. Do not use as a power supply function when connected to GND.

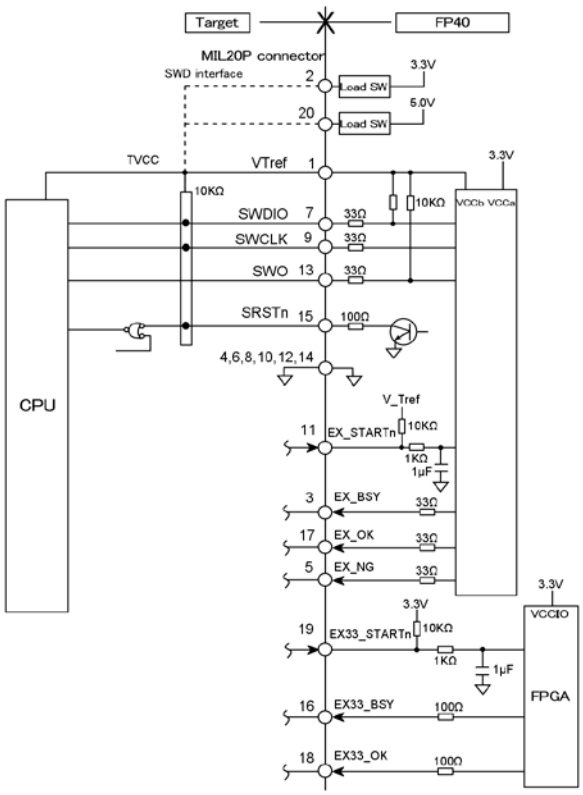
*1: Input/output is based on the target system.

Signal table

Pin No.	Signal	Input/ Output *1	Pin No.	Signal	Input/ Output *1
1	VTref	Output	2	[X3.3V] *5	Input
3	(EX_BSY)*2	Input	4	GND	
5	(EX_NG)*2	Input	6	GND	
7	SWDIO	Input/ Output	8	GND	
9	SWCLK	Input	10	GND	
11	(EX_STARTn)*2	Output	12	GND	
13	SWO*3	Output	14	GND	
15	SRSTn	Input	16	<EX33_BSY>*4	Input
17	(EX_OK) *2	Input	18	<EX33_OK>*4	Input
19	<EX33_STARTn>*4	Output	20	[X5V] *5	Input

*1: Input/output is denoted for the target system.
*2: External input/output function signal that will be at VTref level when high. This signal is not connected to the target (CPU).
*3: Unused. NC.
*4: 3.3V External input/output function signal. This signal is not connected to the target (CPU).
*5: Power supply function signal.

Target connection reference diagram



- To prevent malfunction, the length of wirings from the CPU to the target connector should be kept as short as possible.
- If the waveform disturbance exceeds the device specifications, suppress the disturbance by inserting a damping resistor into the signal line or use other means.

② JTAG interface

The JTAG interface signal table when connected with a 20-pin 2.54mm pitch connector is shown below.
In addition to the standard JTAG signal, FP-40 provides power supply function and external input/output function by FP-40's original signal.

Signal description

Pin No.	JTAG I/F		FP-40		FP-40 unique Specifications	Connection
	Signal	Input/ Output*1	Signal	Input/ Output*1		
1	VTref	Output	VTref	Output	-	Connect the I/O power supply of the CPU to be connected.
2	TVDD	Output	**X3.3V (N.C.)**	**Input**	**Yes**	TVDD signal is not used in FP-40. X3.3V is a FP-40 unique signal and can be used as 3.3V power supply function. Please note that this signal should not be used if X5V(Pin 20) is used as the power supply. When not used, leave as NC.
3	**$\overline{\text{TRST}}$/ N.C.(Cortex-M)**	-	**$\overline{\text{TRST}}$**	**Input**	-	$\overline{\text{TRST}}$ is not used with Cortex-M core CPUs. Leave as NC. For CPUs other than Cortex-M, please refer to the datasheet.
4	GND	-	GND	-	-	
5	TDI	Input	TDI	Input	-	
6	GND	-	GND	-	-	
7	TMS	Input	TMS	Input	-	
8	GND	-	GND	-	-	
9	TCK	Input	TCK	Input	-	
10	GND	-	GND	-	-	
11	N.C.	-	N.C.	-	-	
12	GND	-	GND	-	-	
13	TDO	Output	TDO	Output	-	
14	GND	-	GND	-	-	
15	SRSTn	Input	SRSTn	Input	-	Connect the reset signal to the connected CPU with a wired OR circuit or an OR circuit. The SRSTn signal is an open collector output.
16	GND	-	**EX33_BSY (N.C.)**	Input	**Yes**	EX33_BSY is an FP-40 original signal and outputs the operation status from FP-40. When not used, leave as NC.
17	N.C.	-	N.C.	-	-	
18	GND	-	**EX33_OK (N.C.)**	Input	**Yes**	EX33_OK is an FP-40 original signal and outputs the operation status from FP-40. When not used, leave as NC.
19	N.C.	-	**EX33_STARTn (N.C.)**	Output	**Yes**	EX33_STARTn is an FP-40 original signal and can be used as a write start request signal to FP-40. When not used, leave as NC.
20	GND	-	**X5V (N.C.)**	Input	**Yes**	X5V is FP-40's unique signal and can be used as 5V power supply function. Cannot be used with 2-pin 3.3V power supply. If not used, leave as NC. Do not use as a power supply function when connected to GND.

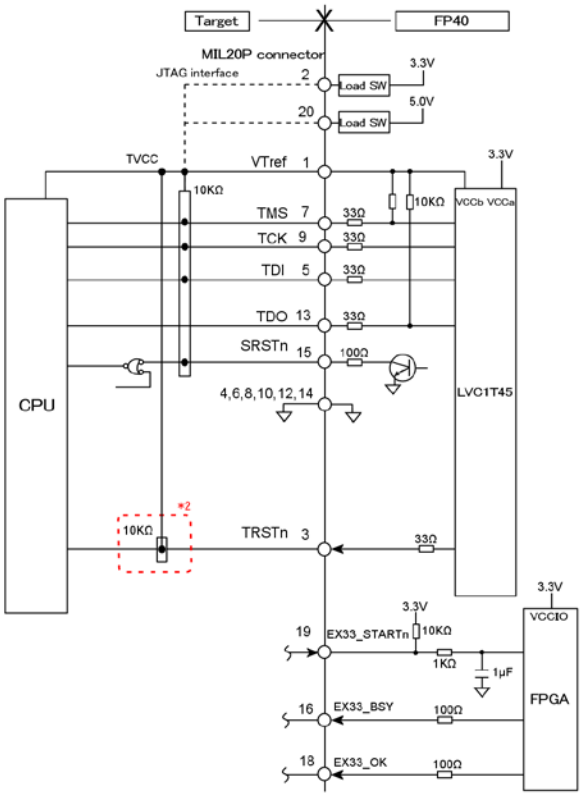
*1: Input/output is based on the target system.

Signal table

Pin No.	Signal	Input/ Output *1	Pin No.	Signal	Input/ Output *1
1	VTref	Output	2	[X3.3V] *4	Input
3	$\overline{\text{TRST}}$ (N.C.) *2	Input	4	GND	
5	TDI	Input	6	GND	
7	TMS	Input	8	GND	
9	TCK	Input	10	GND	
11	N.C. *2	Output	12	GND	
13	TDO	Output	14	GND	
15	SRSTn	Input	16	<EX33_BSY> *3	Input
17	N.C. *2	Input	18	<EX33_OK> *3	Input
19	<EX33_STARTn> *3	Output	20	[X5V] *4	Input

*1: Input/output denoted is for the target system.
*2: $\overline{\text{TRST}}$ TRST is not used with Cortex-M core CPUs. Leave as NC. For other CPUs, please refer to the datasheet of the CPU to be connected.
Please note that CPUs that require connection may require the signals to be pulled-down.
Note that some CPUs manufactured by Renesas Electronics require some precautions. Refer to "Reference：RZ/A and RZ/T series /SRST, /TRST reference diagram" below.
*3: 3.3V External input/output function signal. This signal is not connected to the target (CPU).
*4: Power supply function signal.
*5: Reserved for FP-40's own usage, leave as NC.

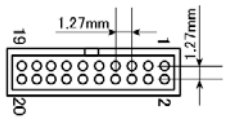
Target connection reference diagram



- To prevent malfunction, the length of wirings from the CPU to the target connector should be kept as short as possible.
- If the waveform disturbance exceeds the device specifications, suppress the disturbance by inserting a damping resistor into the signal line or use other means.

20-pin 1.27mm-pitch connector

Target connector specifications



(Top view on the target board)

Recommended connector
Manufacturer: Samtec, Inc.
Model: FTSH-110-01-L-DV-K
(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please refer the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

③ SWD interface

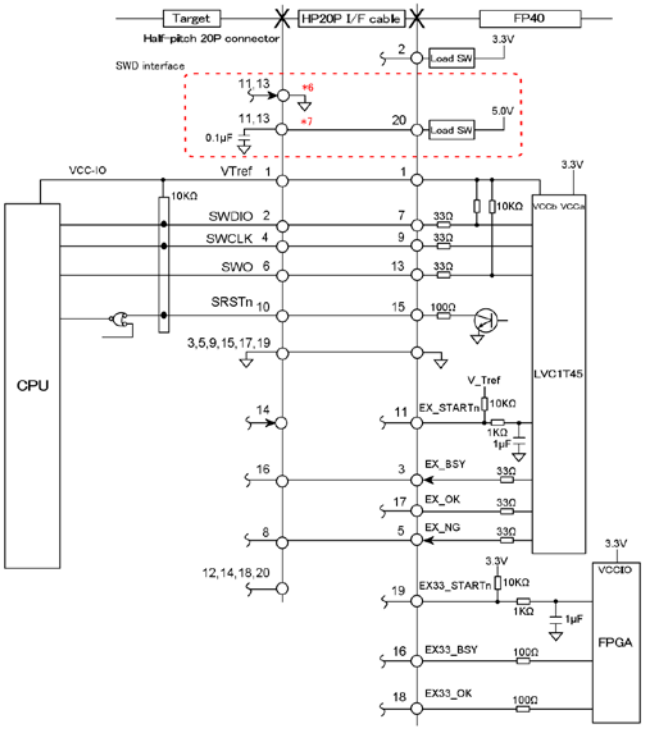
The signal table and target connection reference diagram when connecting a 20-pin 1.27mm pitch connector with SWD interface are shown below.

Signal table

Pin No.	Signal	Input/ Output *1	Pin No.	Signal	Input/ Output *1
1	VTref*2	Output	2	SWDIO	Input/ Output
3	GND		4	SWCLK	Input
5	GND		6	SWO*3	Output
7	Key*5		8	NC	NC
9	GND		10	SRSTn*4	Input
11	GND*6/TgtPwr*7		12	TraceClk*3	Output
13	GND*6/TgtPwr*7		14	TraceD0*3	Output
15	GND		16	TraceD1*3	Output
17	GND		18	TraceD2*3	Output
19	GND		20	TraceD3*3	Output

*1: Input/output is denoted for the target system.
*2: Connect the I/O power supply of the CPU to VTref.
*3: Unused. NC.
*4: Connect the reset signal to the connected CPU with a wired OR circuit or an OR circuit. The SRSTn signal is an open collector output.
*5: Intended for protection against erroneous insertion.
*6: If SWJ-PRB-MIL20-20HP is used, this can be left as NC
*7: If SWJ-PRB-MIL20-20HP-P5V is used, the power supply function of FP can be used. If the power supply function is not used, leave the pins as NC.

Target connection reference diagram



- To prevent malfunction, the length of wirings from the CPU to the target connector should be kept as short as possible.
- If the waveform disturbance exceeds the device specifications, suppress the disturbance by inserting a damping resistor into the signal line or use other means.

④ JTAG interface

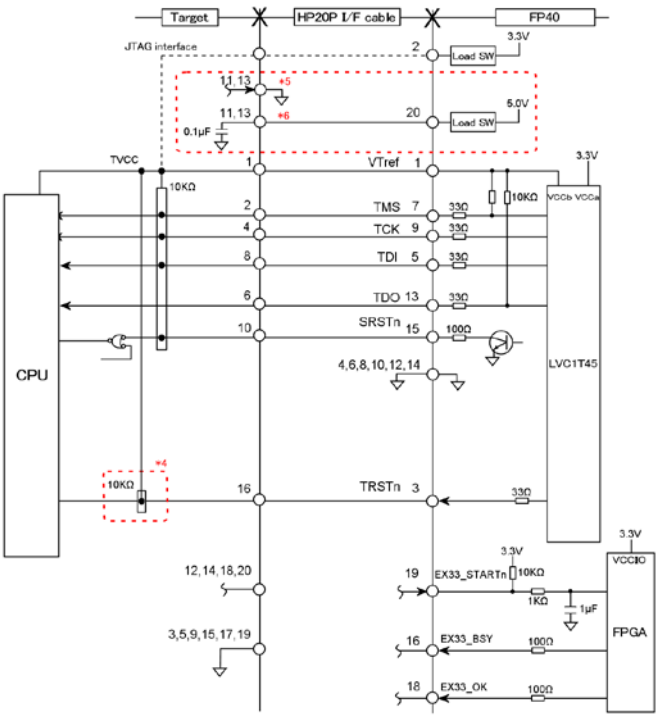
The signal table and target connection reference diagram when connecting a 20-pin 1.27mm pitch connector with JTAG interface are shown below.

Signal table

Pin No.	Signal	Input/ Output *1	Pin No.	Signal	Input/ Output *1
1	VTref	Output	2	TMS	Input
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key*3		8	TDI	Input
9	GND		10	$\overline{\text{SRST}}$*2	Input
11	GND*5/TgtPwr*6		12	NC	
13	GND*5/TgtPwr*6		14	NC	Output
15	GND		16	$\overline{\text{TRST}}$*4	Input
17	GND		18	NC	
19	GND		20	NC	

*1: Input/output is denoted for the target system.
*2: $\overline{\text{SRST}}$ is an open drain output signal.
Connect to the target system's "power-on reset" or "system reset" with a wired OR circuit or, if a wired OR circuit is not possible, with an OR circuit. VCC should be connected to a power supply matching the circuitry of the target system at 5 V or less.
*3: Intended for protection against erroneous insertion.
*4: $\overline{\text{TRST}}$ is not used with Cortex-M core CPUs. Leave as NC. For other CPUs, please refer to the datasheet of the CPU to be connected.
Please note that CPUs that require connection may require the signals to be pulled-down.
Note that some CPUs manufactured by Renesas Electronics require some precautions. Refer to "Reference：RZ/A and RZ/T series /SRST, /TRST reference diagram " below.
*5: If SWJ-PRB-MIL20-20HP is used, this can be left as NC
*6: If SWJ-PRB-MIL20-20HP-P5V is used, the power supply function of FP can be used. If the power supply function is not used, leave the pins as NC.

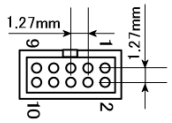
Target connection reference diagram



■ To prevent malfunction, the length of wirings from the CPU to the target connector should be kept as short as possible.

10-pin 1.27mm-pitch connector

Target connector specifications



(Top view on the target board)

Recommended connector
Manufacturer: Samtec, Inc.
Model: FTSH-105-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please refer the pin configuration diagram above and make sure that the connector is in the right direction before connecting.
Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

This connector does not support the power supply function to the target.

⑤ SWD interface

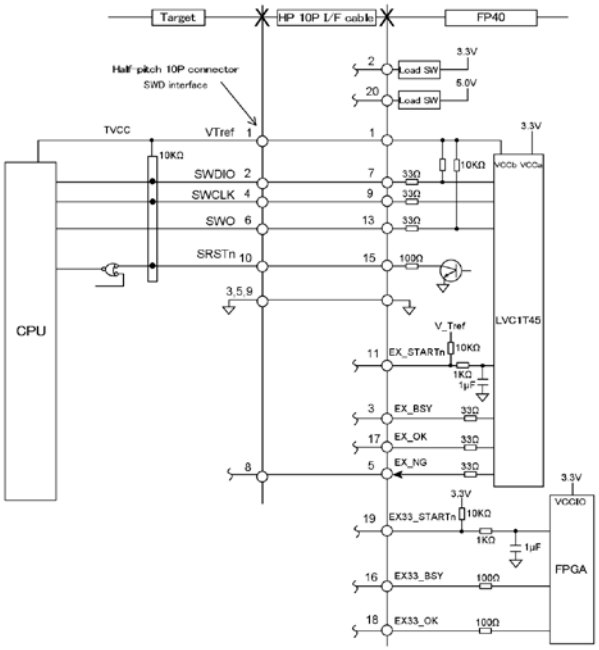
The signal table and target connection reference diagram when connecting a 10-pin 1.27mm pitch connector with SWD interface are shown below.

Signal table

Pin No.	Signal	Input/ Output *1	Pin No.	Signal	Input/ Output *1
1	VTref*2	Output	2	SWDIO	Input/ Output
3	GND		4	SWCLK	Input
5	GND		6	SWO*3	Output
7	Key*5		8	NC	Input
9	GND		10	SRSTn*4	Input

*1: Input/output is denoted for the target system.
*2: Connect the I/O power supply of the CPU to VTref.
*3: Unused. NC.
*4: Connect the reset signal to the connected CPU with a wired OR circuit or an OR circuit. The SRSTn signal is an open collector output.
*5: Intended for protection against erroneous insertion.

Target connection reference diagram



■ To prevent malfunction, the length of wirings from the CPU to the target connector should be kept as short as possible.
■ If the waveform disturbance exceeds the device specifications, suppress the disturbance by inserting a damping resistor into the signal line or use other means.

⑥ JTAG interface + Trace

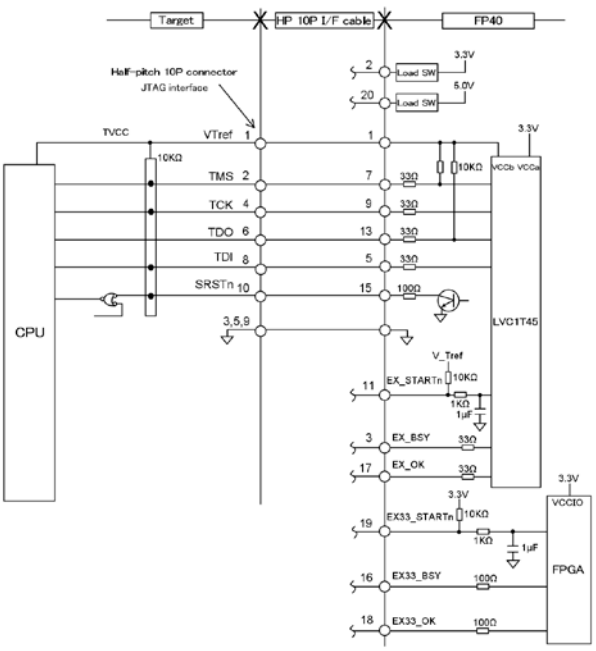
The signal table and target connection reference diagram when connecting a 10-pin 1.27mm pitch connector with JTAG interface are shown below.

Signal table

Pin No.	Signal	Input/ Output *1	Pin No.	Signal	Input/ Output *1
1	Vtref	Output	2	TMS	Input
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key*3		8	TDI	Input
9	GND		10	SRSTn*2	Input

*1: Input/output is denoted for the target system.
*2: Connect the reset signal to the connected CPU with a wired OR circuit or an OR circuit. The SRSTn signal is an open collector output.
*3: Intended for protection against erroneous insertion.

Target connection reference diagram



- To prevent malfunction, the length of wirings from the CPU to the target connector should be kept as short as possible.
- If the waveform disturbance exceeds the device specifications, suppress the disturbance by inserting a damping resistor into the signal line or use other means.

SWD/JTAG(Cortex core)

Refer to the interface specifications below to connect to the target.

FP-40 target interface specifications(SWD/JTAG Cortex)

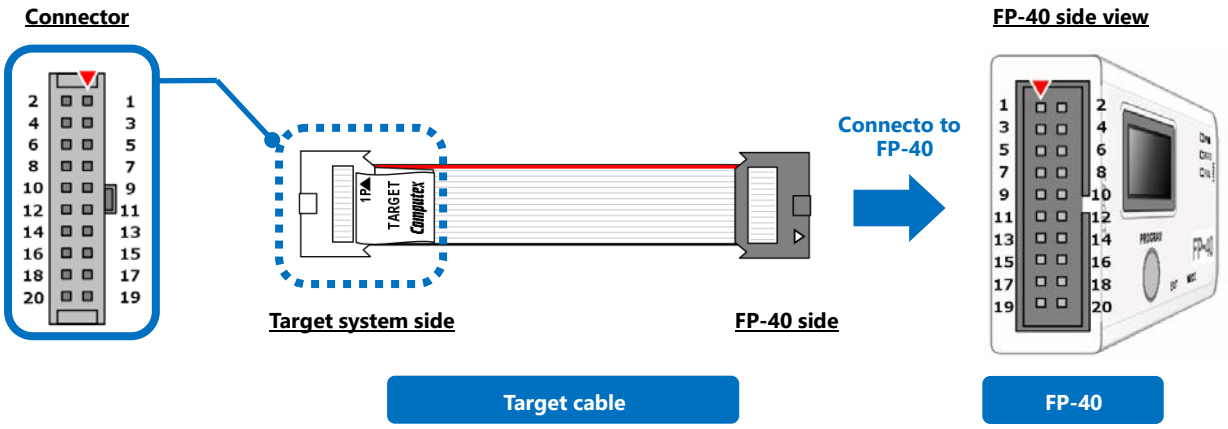
This chapter describes the target interface specifications for connecting FP-40 to the target.

Specifications of the target connector

The standard interfaces supported by FP-40 are JTAG and SWD, and the connector specification is MIL 20-pin with 2.54mm pitch. Connection to the target system is made using the supplied dedicated interface cable (TARGET cable). For interfaces other than JTAG and SWD, please refer to their individual instruction manuals.

Pin allocation

The pin allocations are specific to FP-40 and the target cable is dedicated to FP-40. Make sure that you only use the TARGET cable that is included with the product.

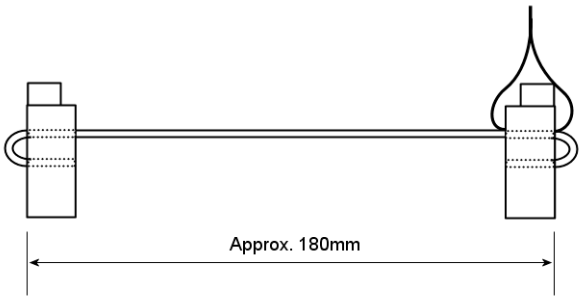


No.	Signal *1	Input/ Output *2	FP-40 internal circuit	access point		
				20-pin 2.54mm-pitch	20-pin 1.27mm-pitch	10-pin 1.27mm-pitch
1	VTref	Output	4KΩPull-Down	1	1	1
2	X3.3V	Input	Power supply (when output is permitted)	2	-	-
3	$\overline{\text{TRST}}$ / (EX_BSY)	Input	22Ωseries	3	16	-
4	GND		GND	4,6,8,10,12,14	3,5,9,11,13,15,17,19	3,5,9
5	TDI / (EX_NG)	Input	22Ωseries	5	8	8
6	GND		GND	4,6,8,10,12,14	3,5,9,11,13,15,17,19	3,5,9
7	TMS/SWDIO	Input / Input/Output	22Ωseries 10KΩPull-Up (VTref)	7	2	2
8	GND		GND	4,6,8,10,12,14	3,5,9,11,13,15,17,19	3,5,9
9	TCK/SWCLK	Input	22Ωseries	9	4	4
10	GND		GND	4,6,8,10,12,14	3,5,9,11,13,15,17,19	3,5,9
11	(EX_STARTn)	Output	1KΩseries 10KΩPull-Up (VTref)	11	-	-
12	GND		GND	4,6,8,10,12,14	3,5,9,11,13,15,17,19	3,5,9
13	TDO/SWO	Output	22Ωseries 10KΩPull-Up (VTref)	13	6	6
14	GND		GND	4,6,8,10,12,14	3,5,9,11,13,15,17,19	3,5,9
15	SRSTn	Input	100Ωseries Open-collector output	15	10	10
16	(EX33_BSY)	Input	100Ωseries	16	3,5,9,11,13,15,17,19	3,5,9
17	(EX_OK)	Input	22Ωseries	17	-	-
18	(EX33_OK)	Input	100Ωseries	18	3,5,9,11,13,15,17,19	3,5,9
19	(EX33_STARTn)	Output	1KΩseries 10KΩPull-Up (3.3V)	19	-	-
20	(X5V)	Input	Power supply (when output is permitted)	20	-	-

*1 : Signal names in parentheses ( ) are signals with FP-40's unique specifications.
*2 : Input/Output is based on the target system.

Dimensions of TARGET cable

Dimensions of the dedicated TARGET cable are as follows.



Target interface voltage level

■ Input voltage level

Target voltage (V)	5.0V	3.3V	1.8V
VIH(min)	3.5V	2.0V	1.17V
VIL(max)	1.5V	0.8V	0.63V

■ Output voltage level

Target voltage (V)	4.5V	3.0V	1.65V
VOH(min)	3.8V	2.4V	1.2V
VOL(max)	0.55V	0.55V	0.45V

Signal specifications

JTAG/SWD signals (TCK, TMS, TDI, TDO, SWDIO and SWCLK)

FP-40 communicates with the on-chip debug unit in the ARM core via the JTAG or SWD connections.
JTAG uses four signal lines - TCK, TMS, TDI and TDO, while SWD required two - SWDIO and SWCLK. The signal designation may differ slightly depending on the CPU, but generally for CPUs that use both JTAG and SWD, TMS and SWDIO, TCK and SWCLK use the same terminals.
Make sure to check the specifications of the target CPU before connecting the necessary signals.
Please note that $\overline{\text{TRST}}$ (reset signal for JTAG) is not used.

$\overline{\text{SRST}}$ signal

$\overline{\text{SRST}}$ signal is used as the reset signal for initializing the CPU from FP-40.
The output from FP-40 is open-collector to allow wired-OR connections on the power-on-reset and system reset signals on the target.
Please refer to the CPU datasheet, etc., as the CPU may have its own extensions. Please be especially careful with Renesas CPUs.

$\overline{\text{TRST}}$ signal

Reset signal to initialize the CPU JTAG from FP-40.
If SWD is used, there is no need to connect this signal. Also, with Cortex-M core CPUs, even if you are using JTAG, you do not need to connect $\overline{\text{TRST}}$.
Please refer to the CPU datasheet, etc., for $\overline{\text{TRST}}$connections, as they may have been uniquely extended by the CPU. Please be especially careful with Renesas CPUs. The output from the FP-40 is an open collector output to allow wired OR with the target system's power-on reset or system reset signal.

Since the $\overline{\text{TRST}}$signals of SWJ-PRB-MIL20-10HP and FP-40 are not connected, it is necessary to make your own cable for "10-pin connector 1.27mm pitch" connection on CPUs that require $\overline{\text{TRST}}$.

VTref signal

Connect the CPU's I/O power to this signal. The valid range should be 1.65V~5.5V.
FP-40 communicates at a signal level that follows the potential connected to this signal. However, some of FP-40 unique signals are 3.3V dedicated I/F. For specifications, refer to "External I/O functions of FP-40".

X3.3V/X5V power supply

This can be used as the power supply from FP-40 to the target system. The two pins of the target connector are X3.3V (3.3V) and the 20 pins are X5V (5V), both of which guarantee ±5% accuracy and can supply up to 200mA. The rise time upon power-on is 2ms. 3.3V or 5V can be used depending on the C-Flash setting, but they can't be used simultaneously. For details on the settings, refer to "**4.3 Target Settings**" in "**Onboard Flash Memory Programmer FP User's Manual**". These power supplies are equipped with a protection circuit that cuts the power supply if an overcurrent is detected due to a short circuit on the target. To confirm that power is normally supplied to the target, the voltage of VTref is measured by software processing after power is supplied, and if the voltage of VTref is lower than the **[minimum input voltage of VTref (Pin 1)]**, the power output is stopped to protect FP-40 itself.
If these pins are not used, leave them as NC.

External I/O function signals

These signals are for the FP-40's external I/O functions. EX_BSY, EX_NG, EX_STARTn, EX_OK, EX33_BSY, EX33_OK, and EX33_STARTn are assigned to the target connector respectively. The target connector signals are normally connected to the target system in which the CPU to be written is mounted, but these signals are intended to be connected to an external production system or other controller device that controls FP-40. Please refer to “External I/O functions of FP-40” for detailed specifications.
If the External I/O functions of FP-40 is not used, leave these signals as NC.

The specifications are the same as those of the conventional FP-10 model.

UART

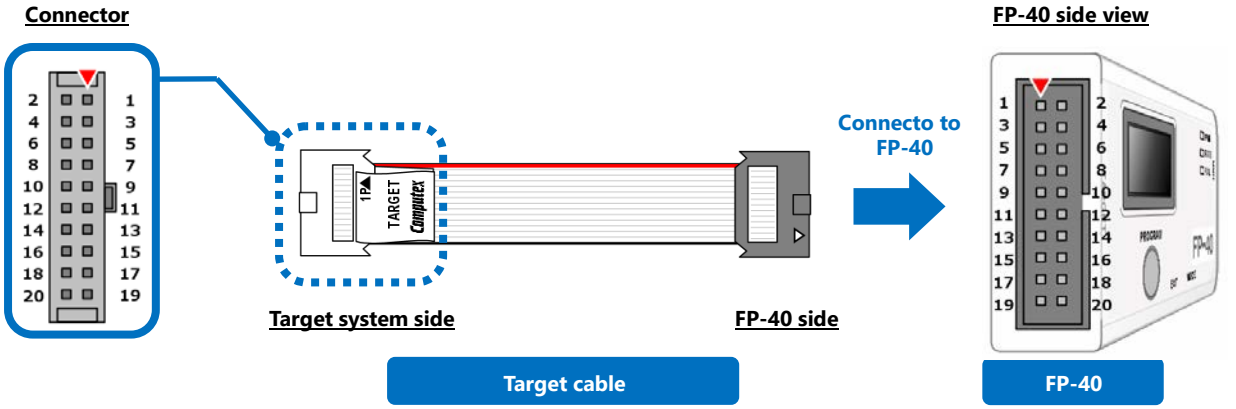
A dedicated cable is not provided to use UART.
Refer to the interface specifications below to connect to the target.

Target interface specifications when using UART on the FP-40 unit

This section describes the interface specifications on the FP-40 unit for connecting the FP-40 to a UART on the target on the.

Specifications of the target connector

Pin allocation



No.	Signal *1	Input/ Output *2	FP-40 internal circuit	access point 20-pin 2.54mm-pitch
1	VTref	Output	4KΩPull-Down	1
2	X3.3V	Input	Power supply (when output is permitted)	2
3	N.C.	Input	22Ωseries	3
4	GND		GND	4,6,8,10,12,14
5	N.C.	Input	22Ωseries	5
6	GND		GND	4,6,8,10,12,14
7	**See [Appendix 1].**			
8	GND		GND	4,6,8,10,12,14
9	**See [Appendix 1].**			
10	GND		GND	4,6,8,10,12,14
11	N.C.	Output	1KΩseries 10KΩPull-Up (VTref)	11
12	GND		GND	4,6,8,10,12,14
13	N.C.	Output	22Ωseries 10KΩPull-Up (VTref)	13
14	GND		GND	4,6,8,10,12,14
15	SRSTn	Input	100Ωseries Open-collector output	15
16	(EX33_BSY)	Input	100Ωseries	16
17	**See [Appendix 1].**			
18	(EX33_OK)	Input	100Ωseries	18
19	(EX33_STARTn)	Output	1KΩseries 10KΩPull-Up (3.3V)	19
20	(X5V)	Input	Power supply (when output is permitted)	20

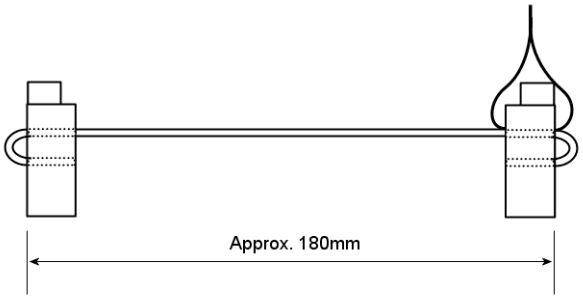
*1 : Signal names in parentheses ( ) are signals with FP-40's unique specifications.
*2 : Input/Output is based on the target system.

[Appendix 1]

No.	MD terminal is used				MD terminal not used				FP-40 internal circuit	access point
	Target side		FP side		Target side		FP side			20-pin 2.54mm -pitch
	signal name	Input/ Output	signal name	Input/ Output	signal name	Input/ Output	signal name	Input/ Output		
7	TXD	Output	RXD	Input	RXD	Input	TXD	Output	22Ωseries 10KΩPull-Up (VTref)	7
9	RXD	Input	TXD	Output	TXD	Output	RXD	Input	22Ωseries	9
17	MODE	Input	MODE	Output	N.C.				22Ωseries	17

Dimensions of TARGET cable

Dimensions of the dedicated TARGET cable are as follows.



Target interface voltage level

■ Input voltage level

Target voltage (V)	5.0V	3.3V	1.8V
VIH(min)	3.5V	2.0V	1.17V
VIL(max)	1.5V	0.8V	0.63V

■ Output voltage level

Target voltage (V)	4.5V	3.0V	1.65V
VOH(min)	3.8V	2.4V	1.2V
VOL(max)	0.55V	0.55V	0.45V

Signal specifications

RXD/TXD signals

UART RXD/TXD signals.

$\overline{\text{SRST}}$ signal

$\overline{\text{SRST}}$ signal is used as the reset signal for initializing the CPU from FP-40.
The output from FP-40 is open-collector to allow wired-OR connections on the power-on-reset and system reset signals on the target.

VTref signal

Connect the CPU's I/O power to this signal. The valid range should be 1.65V~5.5V.
FP-40 communicates at a signal level that follows the potential connected to this signal. However, some of FP-40 unique signals are 3.3V dedicated I/F. For specifications, refer to "External I/O functions of FP-40".

MODE signal

Connect the signal that needs to be controlled when switching CPU boot mode, such as TLCS-870/C1 or RX210. The name of this signal varies depending on the CPU, such as MODE pin or MD pin.
If the CPU is not used, it is N.C.

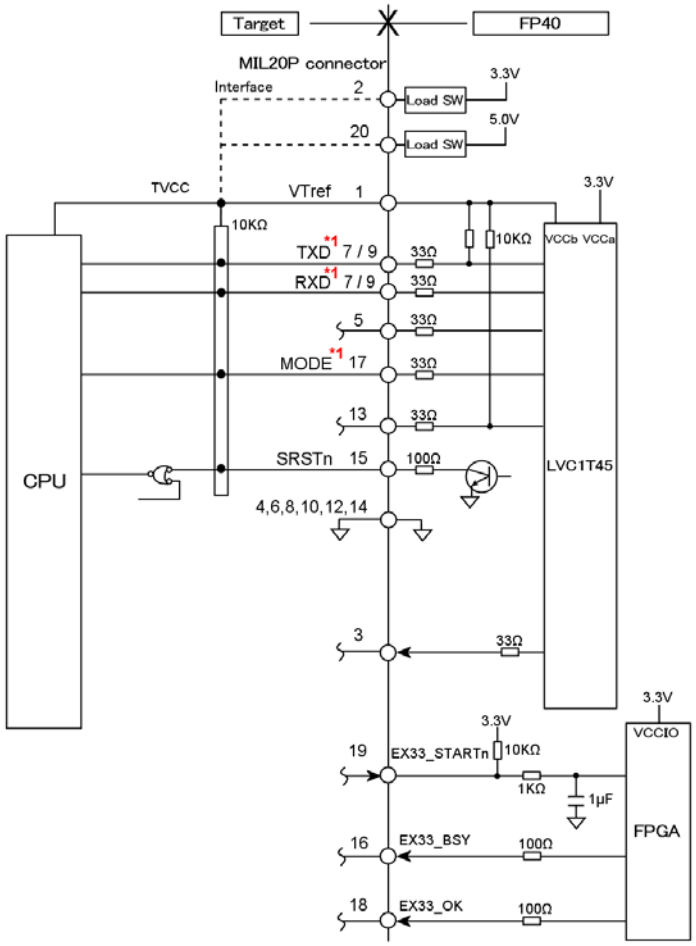
X3.3V/X5V power supply

This can be used as the power supply from FP-40 to the target system. The two pins of the target connector are X3.3V (3.3V) and the 20 pins are X5V (5V), both of which guarantee ±5% accuracy and can supply up to 200mA. The rise time upon power-on is 2ms. 3.3V or 5V can be used depending on the C-Flash setting, but they can't be used simultaneously. For details on the settings, refer to "**4.3 Target Settings**" in "**Onboard Flash Memory Programmer FP User's Manual**".
These power supplies are equipped with a protection circuit that cuts the power supply if an overcurrent is detected due to a short circuit on the target. To confirm that power is normally supplied to the target, the voltage of VTref is measured by software processing after power is supplied, and if the voltage of VTref is lower than the **[minimum input voltage of VTref (Pin 1)]**, the power output is stopped to protect FP-40 itself.
If these pins are not used, leave them as NC.

External I/O function signals of FP-40

Please refer to “External I/O functions of FP-40” for detailed specifications.
If the External I/O functions of FP-40 is not used, leave these signals as NC.
Note that when using UART, external input/output functions (EX_OK, EX_NG, EX_STARTn, EX_BSY) that are powered by VTref (1pin) cannot be used.

Connection reference diagram



*1: By CPU.

Common specifications for each interface

This is a specification of functions that can be used commonly in each interface.

External I/O functions of FP-40

The following signals are provided to allow FP-40 to be operated by an external controller. For information about the Target connector, refer to section "Specifications of the target connector".

External input / output function powered by VTref (1 pin)

This function is available only for SWD interface. It is not available for other interfaces.

Pin No.	Signal	Description	Command
3	EX_BSY*1	Outputs high from FP-40 during writing	FP_EXBSY
5	EX_NG*1	If the write result is NG, high is output from FP-40.	FP_EXNG
11	EX_STARTn*2	Start writing when there is a pulse input to FP-40	FP_EXSTART
17	EX_OK*1	When the write result is OK, H is output from FP	FP_EXOK

*1 : Hi level will be the same as the VTref (Pin 1 of the target connector) level. Level will be L if VTref is cut off.
*2 : Reference voltage needs to be input to VTref in order to detect the pulse.
Note that this function is available only in standalone mode.

The drive capability of the EX_OK, EX_NG, and EX_BSY pins is as follows for both IOL/IOH.

VTref	
1.65~1.95V	4mA
2.3~2.7V	8mA
3.0~3.6V	24mA
4.5~5.5V	32mA

External input / output function using 3.3V I/F

This is provided because when power is supplied to the target system via FP-40, the VTref signal (target voltage) cannot be used as a reference power supply because power is turned on and off in synchronization with the FP-40 writing process.
Note that even when the FP-40 power supply function is not used, it can be used as a normal 3.3V external input/output signal.
However, the external I/O function powered by VTref (Pin 1) above and the 3.3V I/F external I/O function cannot be used together.

Pin No.	Signal	Description	Equivalent signal
16	EX33_BSY	Outputs high from FP-40 during writing	EX_BSY（3 pin）
18	EX33_OK	When the write result is OK, H is output from FP-40	EX_OK（17 pin）
19	EX33_STARTn*1	Start writing when there is a pulse input to FP-40	EX_STARTn（11 pin）

*1 : Note that this function is available only in standalone mode.

The drive capacity of EX33_BSY and EX33_OK is as follows.

Voltage	
3.3 V	12mA

EX_OK/EX33_OK

Three modes of output are available for EX_OK. The presence or absence of the output and the mode switching of the output are performed in C-Flash (see below).

① Result output (High at OK, Low at NG)

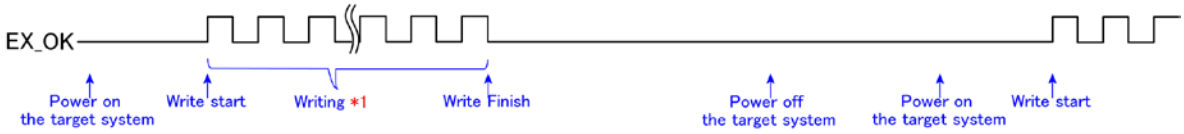
Hi is output when write completes successfully. If writing fails, nothing(L) is output.

② LED interlocking (Pulse output during writing, High at OK, Low at NG)

EX_OK pulse will resemble the turning on and off of the STS LED on the FP.

■ The following waveform is output during Write operation and when the operation completes successfully:

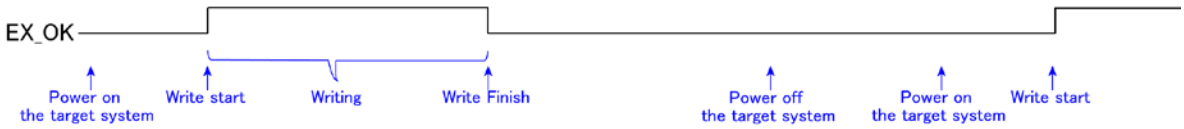
■ The following waveform is output during Write operation and when the Write operation fails:



*1 : Low/Hi signal period may vary during Write operation

③ Write interlocking (High during writing, Low after writing)

Hi is output on EX_OK when Write operation is in progess. After write operation comepletes, irrespective of whether the Write operation succeeds or fails the signal level drops to L.

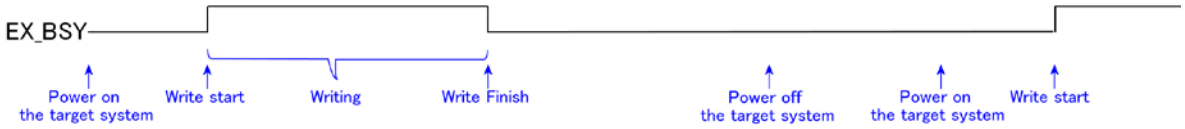


EX_STARTn/EX33_STARTn

EX_STARTn starts writing when an external falling edge is detected on EX_STARTn instead of the **PROGRAM switch**.
To use this function, it must be set in C-Flash (see below).
Please note that edge detection of EX_STARTn signal will be ignored when Write operation is in progress.

EX_BSY/EX33_BSY

To use EX_BSY, it needs to be configured using C-Flash. (see below)。
When EX_BSY is configured, H is output during Write operation and L is output when Write operation completes.
Please note that this signal is shared with the JTAG's $\overline{\text{TRST}}$ signal. Make sure not use this signal when the $\overline{\text{TRST}}$ signal of the CPU on the target system is connected to FP.



EX_NG

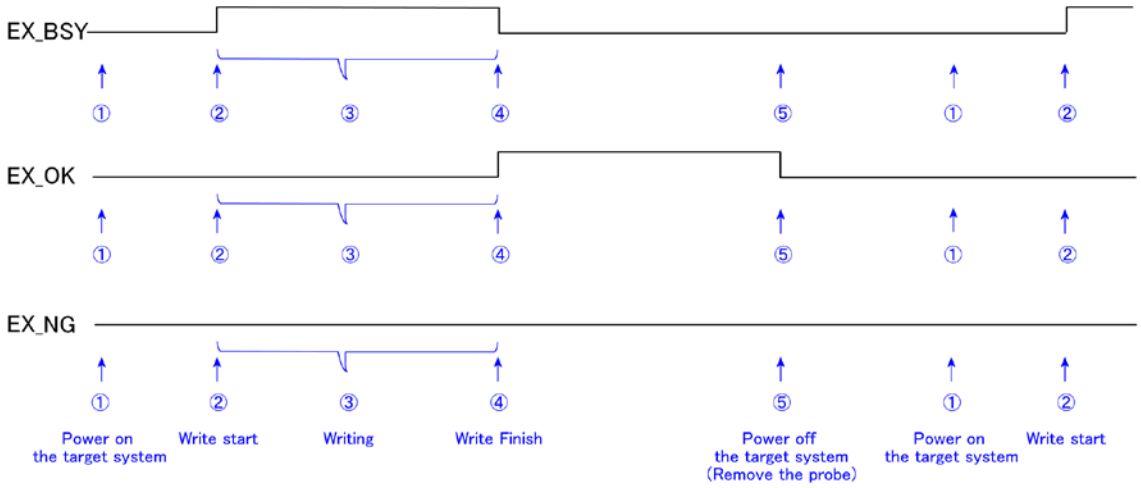
To use EX_NG, it needs to be configured using C-Flash. (see below)。
When EX_NG is configured, H is output when Write operation fails.
Please note that this signal is shared with the JTAG's TDI signal. Make sure not use this signal when the TDI signal of the CPU on the target system is connected to FP.

In External input/output function using 3.3V I/F, no signal is output.

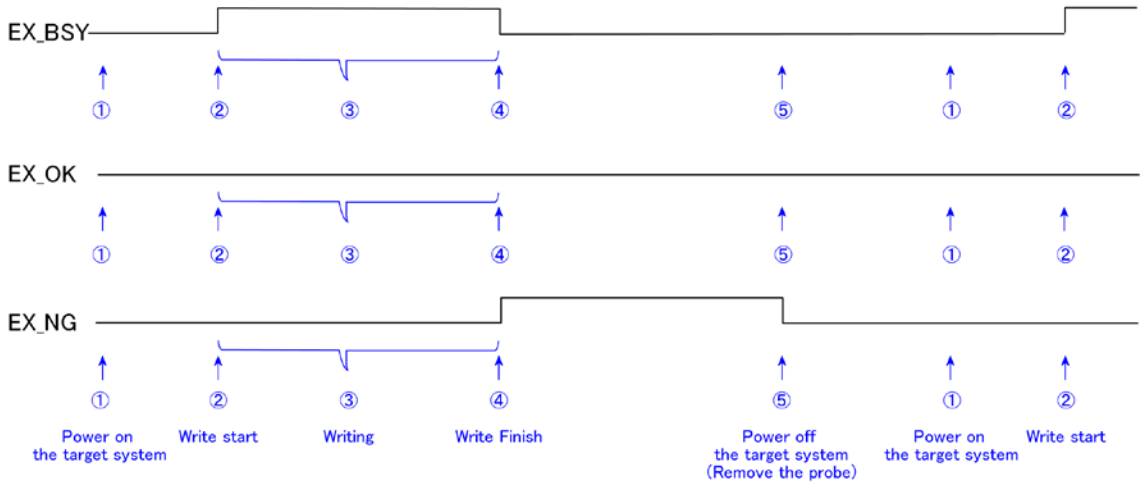
Using each signal in combination

By setting EX_OK signal to "result output" and enabling the output of the EX_BSY and EX_NG signals, the three signals can be combined to determine the progress and result of Write operation with the external device.
This also applies to EX33_OK and EX33_BSY signals of the External input/output function when 3.3V I / F is used.
In External input/output function, EX_NG signal is output using 3.3V I/ F.

- The following waveform is output during Write operation and when the operation completes successfully:

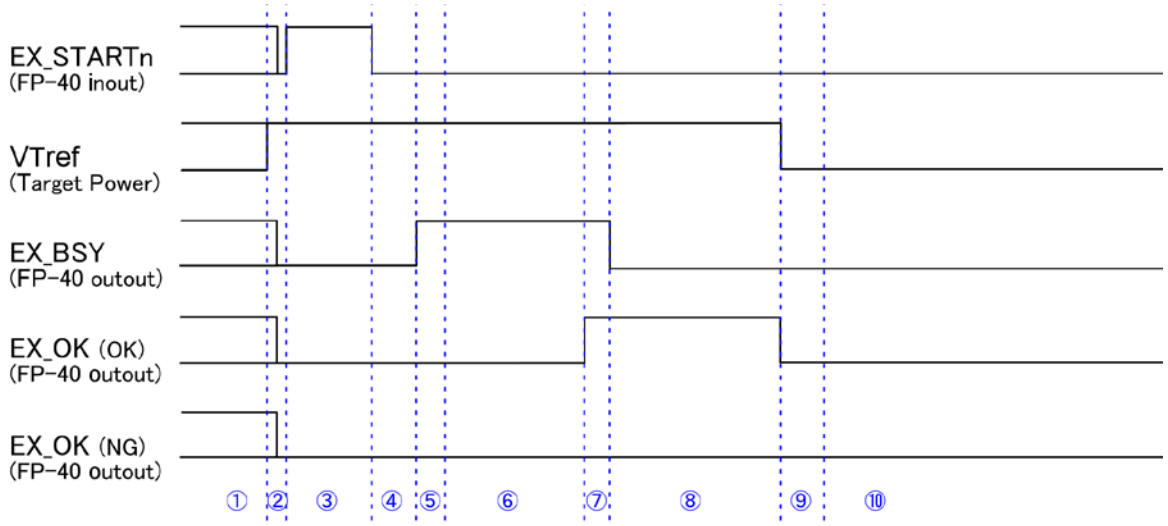


- The following waveform is output during Write operation and when the Write operation fails:



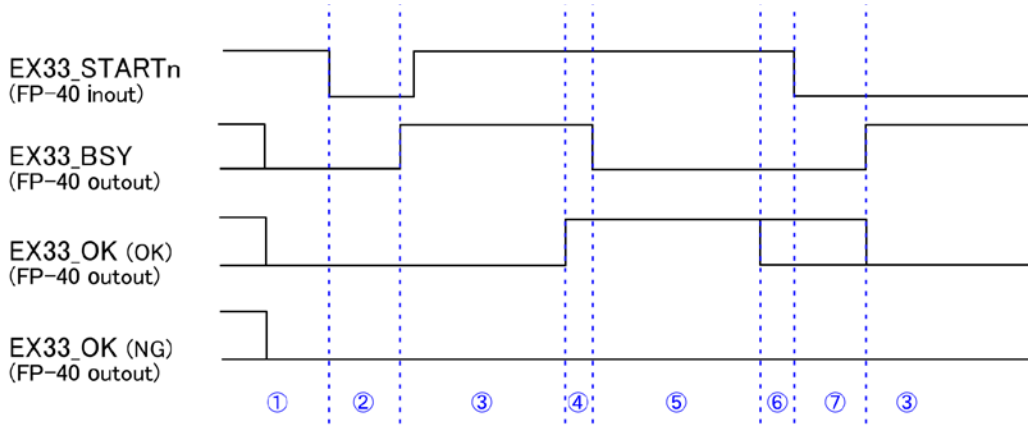
H level will be the same as the VTref (Pin 1 of the target connector) level. The level will be L if Vtref is cut off.
If VTref signal is interrupted, EX_OK/EX_NG signal will automatically output L. H will not be output even if VTref signal is restored after this during the current operation.
In External input/output function using 3.3V I/F, H level will be at 3.3V.
FP-40 monitors if External input/output function is powered by VTref (Pin 1) and if VTref signal is interrupted.

External I / O function timing with VTref (1 pin)



①	FP-40 setup time(4500ms,Only immediately after the FP-40 power supply,Usually ⑩)
②	EX_STARTn goes high after input of Vtref Note that EX_STARTn of FP-40 monitors the falling edge and does not recognize the rising edge.
③	HI retention of EX_STARTn (no specified time)
④	Write processing starts when the EX_STARTn falling edge is detected. (5ms)
⑤	Processing before writing
⑥	Writing
⑦	EX_BSY, EXOK change time
⑧	Result output(OK:EX_OK/HI,NG:EX_OK/LOW)
⑨	After FP-40 power down is detected, transition to next write occurs.
⑩	Waiting for the next start.

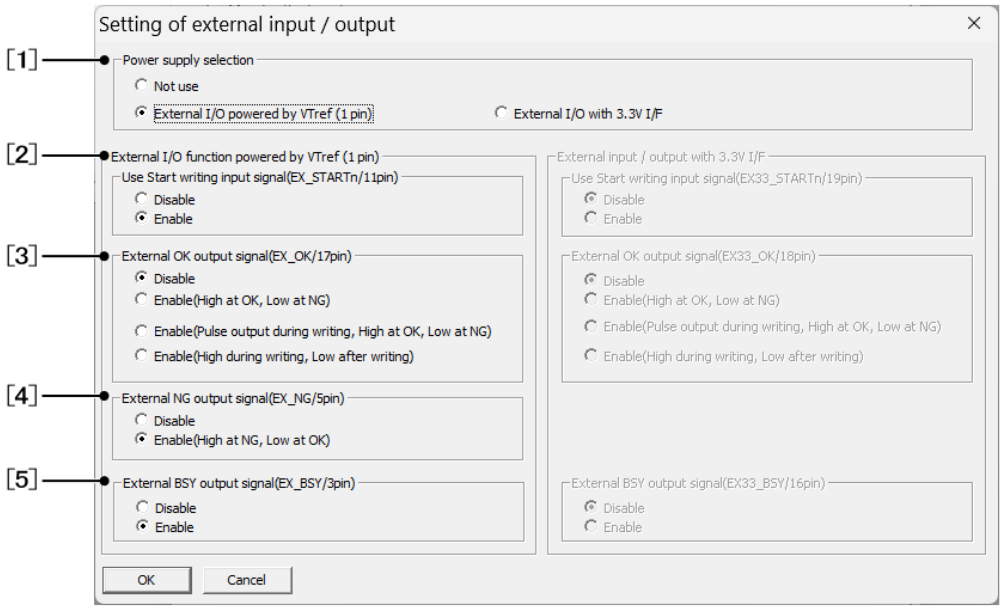
External I / O function timing with 3.3V I/F



①	FP-40 setup time(4500ms,Only immediately after the FP-40 power supply)
②	Write processing starts when EX33_STARTn falling edge is detected. (5ms)
③	Writing
④	EX_BSY, EXOK change time
⑤	Result output(OK:EX_OK/HI,NG:EX_OK/LOW)
⑥	When the power supply function of FP-40 is not used,EX33_OK is LOW when there is no VTref input. When the power supply function of FP-40 is used,EX33_OK keeps HI. Wait time for next write
⑦	When the power supply function of FP-40 is used,EX_STARTn After recognizing the falling edge, set EX33_OK to LOW.

C-Flash Settings

Navigate to **[Target system setting] [Set Initial value]** tab. On clicking the **[External I/O Setting]** button, the following setting screen will be displayed:



[1] Power supply selection

Select whether to use VTref or 3.3V I/F. Both cannot be used simultaneously.

When **[Do not use]** is selected, each signal is automatically set to [Do not use/output].

[2] Use Start writing input signal

Input signal to FP-40 to start the Write procedure.

[Enable] is automatically selected if the power supply is set to enable in the power supply selection.

[3] External OK output signal

Select the output format of the OK signal.

[4] External NG output signal

Selects the output of the NG signal. Note that the 3.3V I/F does not provide a signal equivalent to EX_NG.

[Enable] is automatically selected if the power supply is set to enable in the power supply selection.

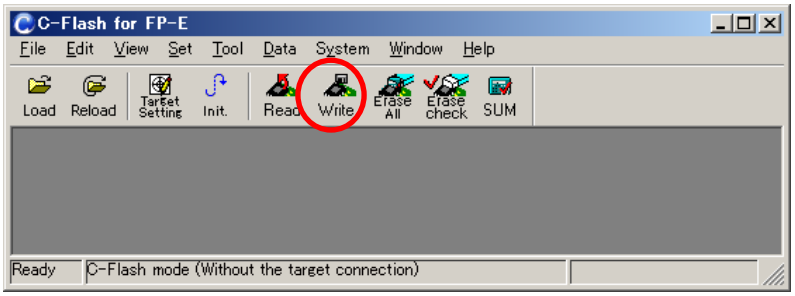
[5] External BSY output signal

Select the output format of the BSY signal.

[Enable] is automatically selected if the power supply is set to enable in the power supply selection.

Press the **[Write]** button to reflect these setting in FP-40 (Otherwise, these settings will not be reflected in Standalone-mode).

If **[Write]** is grayed out and can not be pressed, refer to "4.3 Target System Settings" and "3.2.2 Specifying the data (file) for writing into on-chip flash memory" in "Onboard Flash Memory Programmer FP User's Manual"to make various settings of C-Flash until the **[Write]** button becomes enabled.
Press the **[Write]** button.



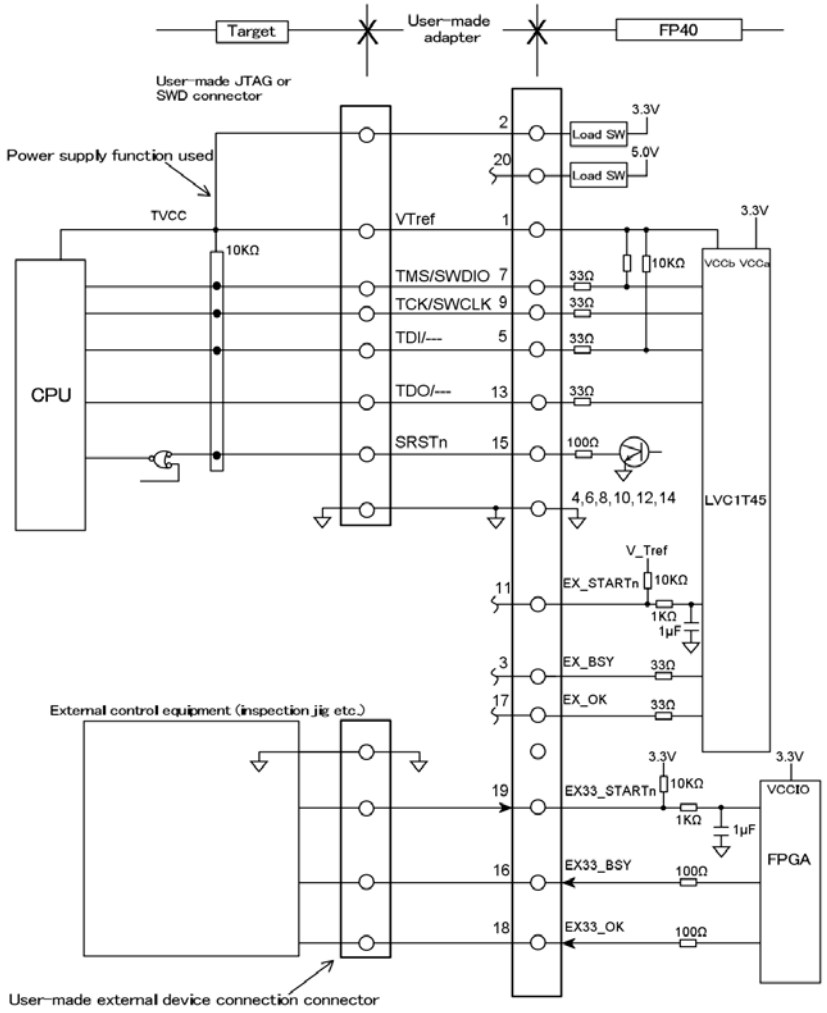
Done.

Note

The external I/O settings are saved in the C-Flash project file. If C-Flash is launched with a project file in which external I/O functions are disabled, and if a [Write] is performed on FP-40 on which external I/O functions are enabled, the external I/O function will be disabled according to the settings in the project file.

Power supply

FP-40 has the ability to supply 3.3V or 5.0V power to the target system up to 200mA (simultaneous use of 3.3V and 5.0V power supplies is not possible.) An example using X3.3V power supply is shown below.

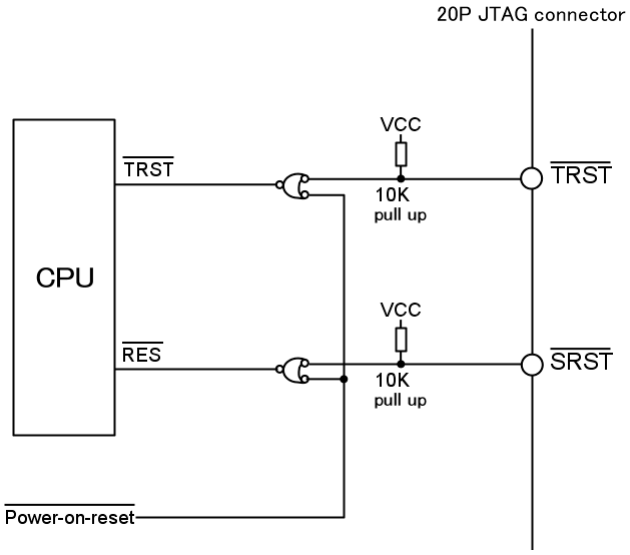


C-Flash settings

The signal output settings are made in the [Power Supply/External Signal] tab of the [Target Settings] in C-Flash. For details, please refer to the "CM1002_On-board_Flash_Programmer_FP_Users_Manual".

CPU-specific supplement

Reference : RZ/A and RZ/T series /SRST, /TRST reference diagram



It may be required to control the $\overline{\text{RES}}$ and $\overline{\text{TRST}}$ CPU pins so that they are in low state at power on. Refer the CPU datasheet for details.

STM32C031C6T6/UART

When using UART with STM32C031C6T6, connect the following signals:

CPU		Function	FP	
Name	No.		Name	No.
PA10	33	RX(INPUT)	TXD(OUTPUT)	9
PA9	21	TX(OUTPUT)	RXD(INPUT)	7
PF2-NRST	10	Reset(INPUT)	SRSTn(OUTPUT)	15

・In addition, you will need to connect GND and VTref (one pin on the FP side).
・For information about the CPU side signals, be sure to refer to the CPU manual.
・For information about the pin numbers for the FP side signals, please refer to “Target interface specifications when using UART on the FP-40 unit”.

Note

- To prevent malfunction, the length of wirings from the CPU to the target connector should be kept as short as possible.
- If the waveform disturbance exceeds the device specifications, suppress the disturbance by inserting a damping resistor into the signal line or use other means.

Technical Information on On-board Flash Programmer FP-40 (Eighth Edition)

Go through the required procedures as stated under Foreign Exchange and Foreign Trade Control Law in exporting (including the case where travellers directly carry) this product or providing this product for residents outside Japan.