Oct. 15, 2019

This document consists of the following contents.

- Technical Information SPI Flash Programmer FP-30 (Second Edition)

  Refer this document before using FP-30.

- FP-30 User's Manual (6th Edition) - (Excerpted version(*))

  This manual describes target interface specifications of FP-30.

  ※ This is an excerpt of "Chapter 8 Target Interface Specifications" and "Chapter 16 External I/O functions of FP-30" from the FP-30 User's Manual.

SPI Flash Programmer FP-30
Technical Information

Second Edition (Oct. 15, 2019)

Table of Contents

Change history

First Edition	Aug. 30, 2019	Initial version
Second Edition	Oct. 15, 2019	"Applicable connector" added the recommended connector model number.

Introduction

This document explains the interface specifications for “On-board connection” method programming.

FP-30 has two connection methods that are used for programing flash memory:

On-board programming

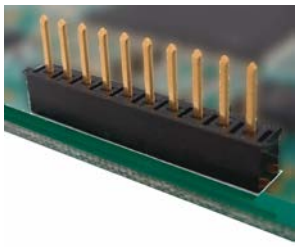
SPI flash memory on a hardware boards can be programmed using this method. The FP unit and the hardware board are connected using an adapter cable.

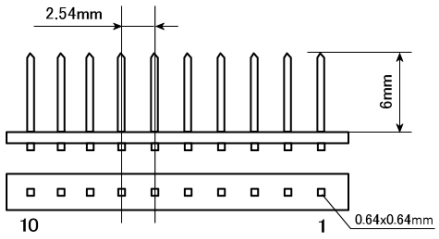
Off-board programming

Individual flash memory chips inserted into a socket adapter can be programmed using this method. A variety of socket adapters for flash memory packages are available to support this operation.

Applicable connector

10 pin 2.54mm pitch connector





(Hardware board connector top view)

※Please refer to the pin layout and be sure to confirm how to assign the pin number.

Recommended connector

Manufacturer : Hirosugi-Keiki Co., Ltd.

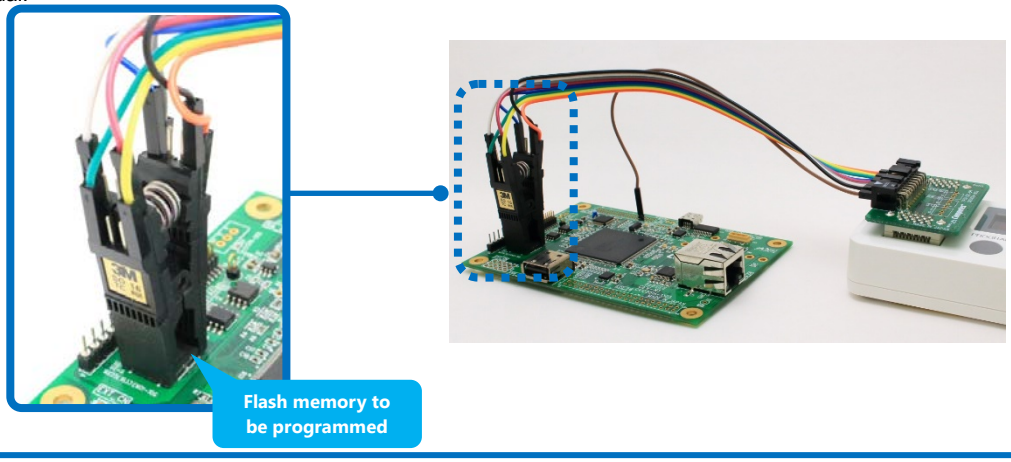
Model : PSS-410153-10

On-board programming example using

For On-board programming, it is recommended to use the adapter cable [**ADP-FP30SA-CBL-S10**] and to use the ISP connector on the target board.

In case of hardware boards that have already been designed/manufactured without an ISP connector, a test clip can be used to program the flash memory.

For details, refer to [Chapter 8 Interfacing with the hardware board (On-board connection)] in the FP-30 User’s Manual.



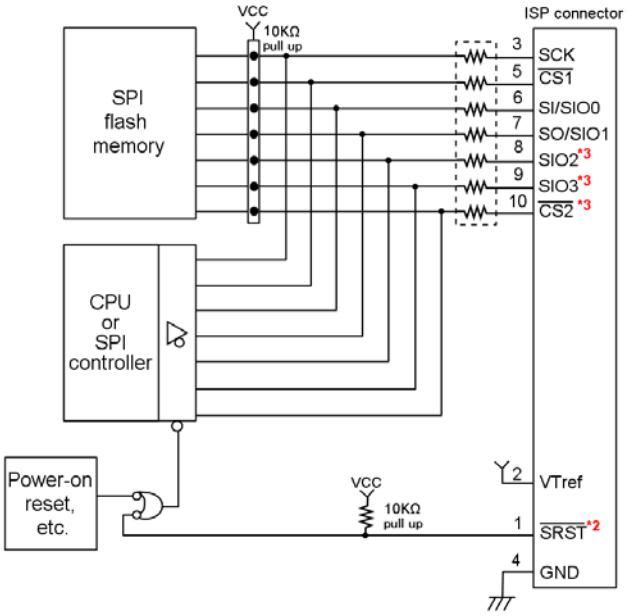
SPI interface signals

Signal table

Pin No.	Signal name	Input/output *1
1	SRST*2	Input
2	VTref	Output
3	SCK	Input
4	GND	-
5	CS1	Input
6	SI/SIO0	Bidirectional
7	SO/SIO1	Bidirectional
8	SIO2*3	Bidirectional
9	SIO3*3	Bidirectional
10	CS2*3	Input

*1: Input/output are determined based on the hardware board side.
*2: The SRST signal is an open collector output.
When this signal is "LOW" on the hardware board, set each SPI signal to high impedance state.
*3: NC if the pins are not used on the flash memory.

Target connection reference diagram



Notes

- Make sure to use the appropriate adapter for FP-30. Operation is only guaranteed if the appropriate adapter is used.
- The wire length between the ISP connector and SPI should be as short as possible. The shorter the better.
- It is recommended to insert a damping resistor between the ISP connector and the SPI flash memory.

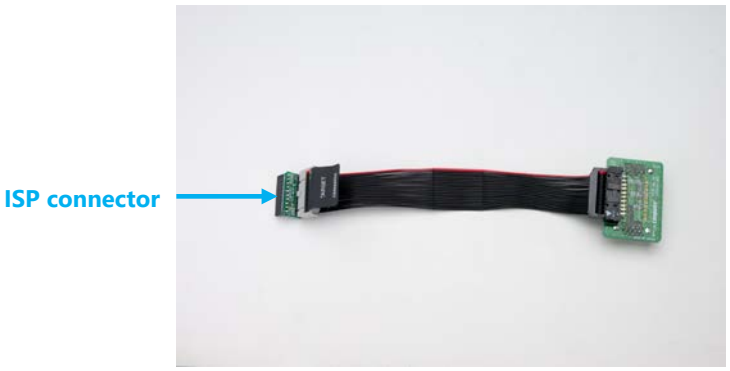
Technical Information on SPI Flash Programmer FP-30 (Second Edition)

Go through the required procedures as stated under Foreign Exchange and Foreign Trade Control Law in exporting (including the case where travellers directly carry) this product or providing this product for residents outside Japan.

Chapter 8 Interfacing with the hardware board (On-board connection)

8.1 Introduction

This chapter explains how to use the adapter cable [ADP-FP30SA-CBL-S10] and program flash memory on a hardware board using On-board connection method.



ADP-FP30SA-CBL-S10 adapter cable

Info.

For technical contents and reference circuits not described in this manual, refer to the manual **[SPI Flash Programmer FP-30 Technical Data]** on our website (https://www.computex.co.jp).

8.2 ISP connector specifications

ISP connector specifications is as follows:

Pin No.	Signal name	Input/output*1	FP-30 internal circuit
1	$\overline{\text{SRST}}$	Input	100Ω series Open collector output
2	Vtref	Output	4KΩ Pull-Down
3	SCLK	Input	22Ω series
4	GND	-	GND
5	$\overline{\text{CS1}}$	Input	22Ω series
6	SI/SIO0	Bidirectional	22Ω series
7	SO/SIO1	Bidirectional	22Ω series
8	SIO2*2	Bidirectional	47Ω series
9	SIO3*2	Bidirectional	22Ω series
10	$\overline{\text{CS2}}$*2	Input	22Ω series

*1 : Input/output are determined based on the hardware board side.
*2 : NC if the pins are not used on the flash memory.

FP-30 side ISP connector
Manufacturer : Hirosugi-Keiki Co., Ltd.
Model : FSS-41085-10

Target side applicable connector
Manufacturer : Hirosugi-Keiki Co., Ltd.
Model : PSS-410153-10
PSS-410156-10

8.2.1 Adapter cable dimensions

The dimensions of the cable type adapter are as follows:

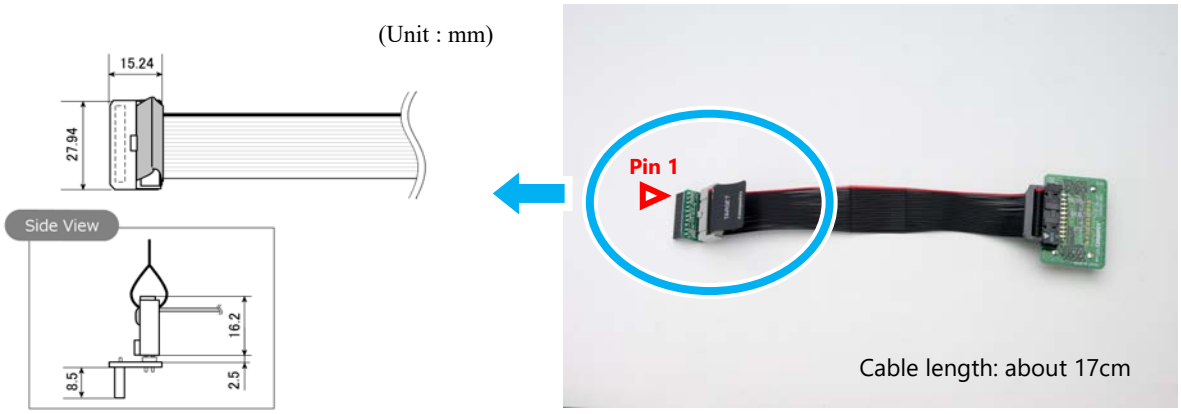


Figure: Target connector dimensions

8.2.2 Signal specifications

The ISP interface signal specifications are explained here:

$\overline{\text{SRST}}$ signal

FP-30 unit outputs a “Low” on this signal to communicate with the SPI flash memory. Make sure that the SPI flash memory signals are in high impedance state on the hardware board. The output from the FP-30 is open collector.

Vtref signal

The flash memory power supply voltage is output on this signal (1.8V~3.3V).

SPI signal (SCLK, $\overline{\text{CS1}}$, SI/SIO0, SO/SIO1, SIO2, SIO3, $\overline{\text{CS2}}$)

These signals are used by the flash memory. NC if not used.

8.3 Electrical characteristics of the target interface

8.3.1 DC characteristics

- SPI signals (SCLK, $\overline{CS1}$, SI/SIO0, SO/SIO1, SIO2, SIO3,$\overline{CS2}$)

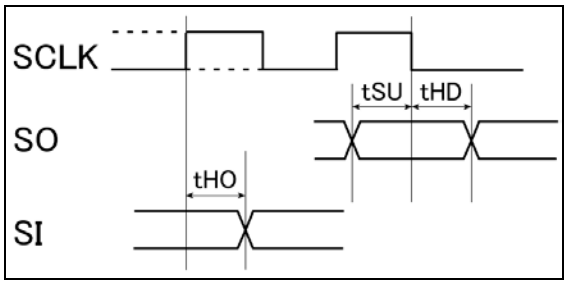
Symbol		Min	Type	Max	Units
VIL (Input Low Voltage)	3.3V			0.8	V
	2.5V			0.7	
	1.8V			0.38	
VIH (Input High Voltage)	3.3V	2.0			V
	2.5V	1.7			
	1.8V	0.8			
VOL (Output Low Voltage)	3.3V			0.4	V
	2.5V			0.4	
	1.8V			0.45	
VOH (Output High Voltage)	3.3V	2.9			V
	2.5V	2.1			
	1.8V	1.35			

* : In the case of On-board connection, the signal/waveform may be disturbed/distorted depending on the length of the wire and load from the FP-30 unit to the SPI flash memory. If the waveform distortion exceeds the device specifications, connect a damping resistor into the signal line to suppress the disturbance.

8.3.2 AC characteristics

- SPI signals (SI/SIO0, SO/SIO1, SIO2, SIO3)

Symbol	Min	Type	Max	Units
tSU (Input Setup Time)	10			ns
tHD (Input Hold Time)	0			ns
tHO (Output Hold Time)	5			ns



8.4 Using a test clip in On-Board connection

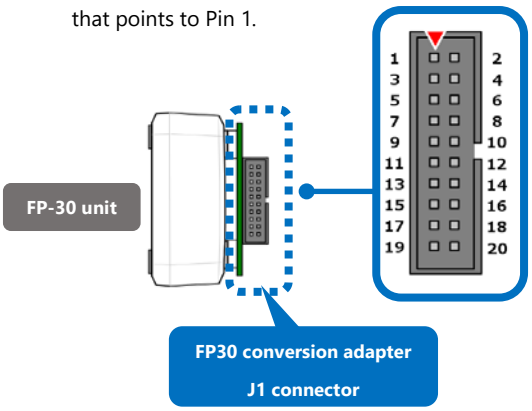
For On-board programming, it is recommended to use the adapter cable **[ADP-FP30SA-CBL-S10]** and to use the ISP connector on the target board.

In case of hardware boards that have already been designed/manufactured without an ISP connector, a test clip can be used to program the flash memory. This procedure is described in this section.

NOTE

It is recommended to use the supplied adapter cable [ADP-FP30SA-CBL-S10] with the ISP connector whenever possible. The method described here is not guaranteed to work always. Incorrect wiring may cause damage to the board or to the flash memory and the FP-30 unit.
Follow this method at your own risk.

The (▼) mark on the connector is not a pointer that points to Pin 1.

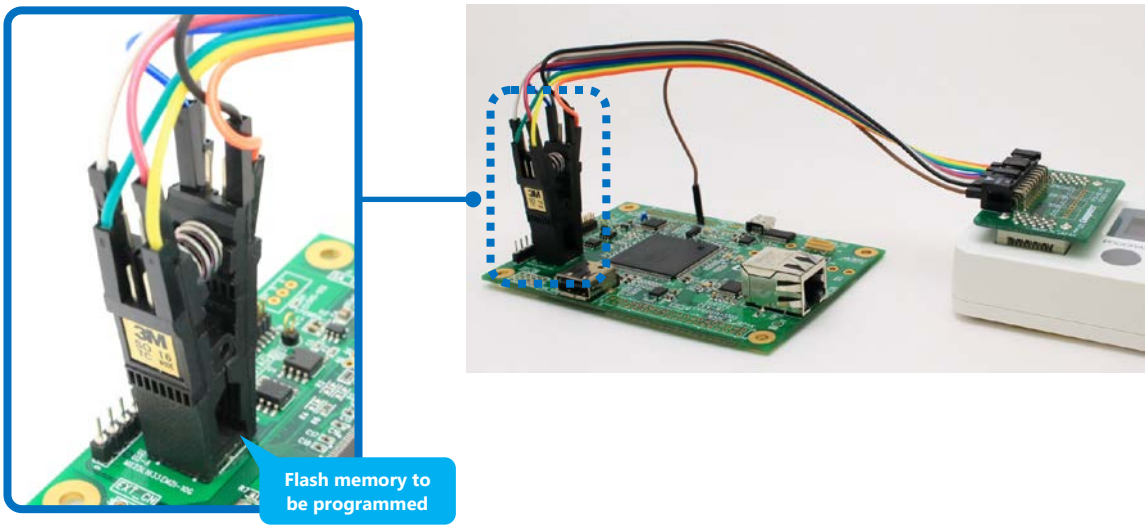


■ FP30 unit conversion adapter [J1 connector] signal table

No.	Signal name	FP-30 Internal circuit	No.	Signal name	FP-30 Internal circuit
1	Vtref	4KΩ Pull-Down	2 *2	(VCCOUT)	Power supply
3	SCLK	22Ω series	4	GND	GND
5	GND	GND	6	GND	GND
7	$\overline{CS1}$	22Ω series	8	GND	GND
9	SI/SIO0	22Ω series	10	GND	GND
11	SO/SIO1	22Ω series	12	GND	GND
13	SIO2 *1	47Ω series	14	GND	GND
15	SIO3 *1	22Ω series	16	GND	GND
17	NC	NC	18	$\overline{CS2}$ *1	22Ω series
19	$\overline{SRST}$	100Ω series Open collector output	20	NC	NC

*1 : NC if the pins are not used on the flash memory.
*2 : VCCOUT (the power output from FP-30) is output regardless of C-Flash settings. Refer section “8.5 Supplying power to target from FP-30”.

In case of SOP 16pin 300mil and SOP 8pin 200mil package flash memory, use a commercially available SOP IC test clip and connect the flash memory and the conversion adapter [J1 connector] of FP-30.



Info.

Tips for connecting

- The cable length between FP-30 and the hardware board should be 20cm or less. The shorter the better.
- The communication is stable at a slower clock speeds.
- Using one I/O data line is stable than using four.
- In additional to SPI signal lines, it is required to connect the $\overline{\text{SRST}}$ (Pin 19: System reset signal). Note that this signal is not the SPI flash reset signal.

8.5 Supplying power to target from FP-30

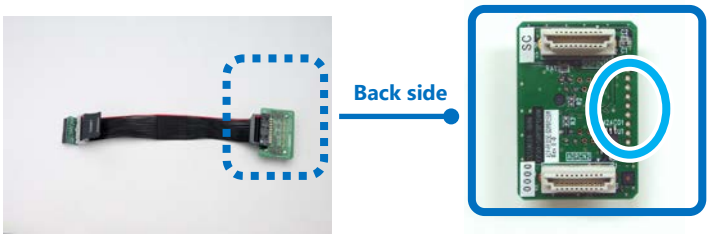
Power can be supplied from FP-30 to the hardware board using the adapter cable **[ADP-FP30SA-CBL-S10] Rev 0-A** and **[C-Flash for SPI] Ver. 1.05.00 or later**. Flash memory on hardware boards with a light load can be written to without having to supply external power.

NOTE

Depending on various factors, some boards might still need an external power supply. Refer to the board manual for details.
Incorrect connection may damage the target board and the FP-30 unit. Follow this method at your own risk.

8.5.1 Check the revision of the adapter cable

Make sure the adapter revision is Rev 0-A before proceeding. The revision can be checked as explained in section **"7.2.2** Hardware revision**".**



8.5.2 Electrical characteristics

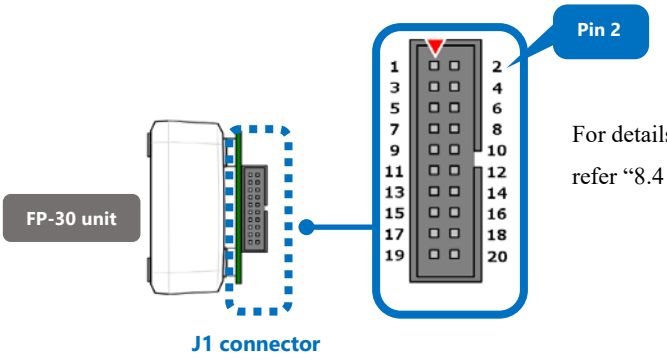
Voltage	1.8V / 2.1V / 2.2V / 2.5V / 2.6V / 2.9V / 3.0V / 3.3V
Current	200mA max

- The option **[Supply power to the target from FP-30]** has to be checked on the "On-board settings tab" of the Detailed settings dialog.
- Ensure that power is supplied to the hardware board only through FP-30 and no other power supply sources are used.
- The current consumption of the hardware board must be less than the max current supported by the FP-30 unit.

8.5.3 Connection points

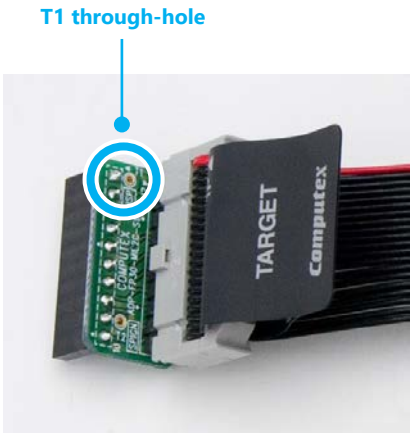
Power can be tapped from the FP-30 unit from these two pins/points:

① FP-30 unit conversion adapter [J1 connector] Pin 2



For details about the **[J1 connector]**,
refer “8.4 Using a test clip in On-Board connection”.

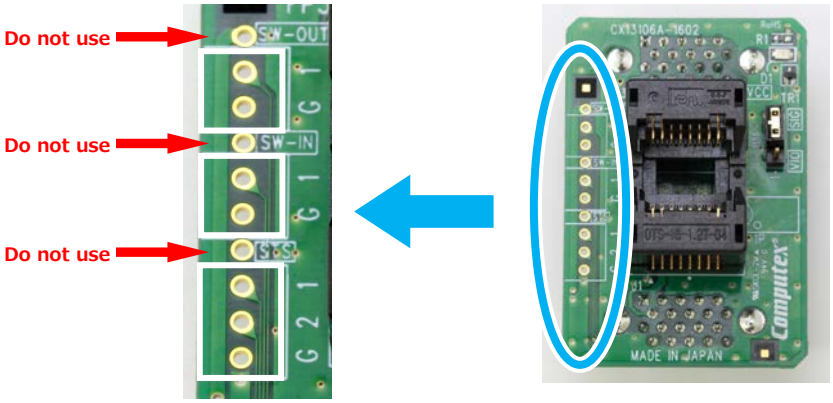
② [T1 through-hole] on the target connector



Chapter 16 External I/O functions

16.1 Introduction

FP-30 units can be controlled from External devices or can be connected in chain fashion. All adapters included with FP-30 have been provided with Input/Output signal terminals for this purpose. Through-holes have been provided for convenient connection.



*** Use only the pins indicated by the white boxes in the picture above. Other pins are not to be used.**

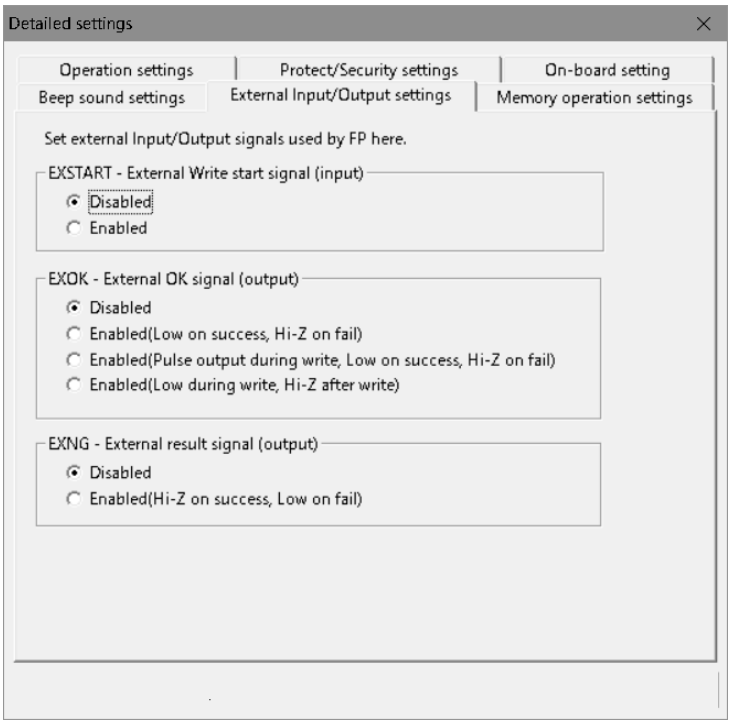
Group name	Pin	Signal name	Input/Output*1	FP-30 internal circuit
SW-OUT	1	EXSTARTOUT	Output	100Ωseries CMOS open drain output
	G	GND		
SW-IN	1	EXSTART	Input	22Ωseries 4.7KΩPull-UP
	G	GND		
STS	1	EXOK	Output	100Ωseries Open collector output
	2	EXNG	Output	100Ωseries Open collector output
	G	GMD		

*1 : Input/output are determined based FP-30 unit side.

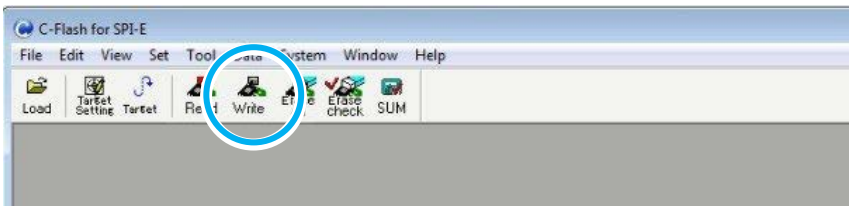
The above signals can be enabled/disabled and the output pattern of EXOK/EXNG can be configured on the **[External Input/Output settings tab]** on the Detailed settings dialog.

16.2 C-Flash settings

External I/O signals have to be configured on the **[External Input/Output settings tab]** on the Detailed settings dialog.



After the settings are done, the **[Write]** button on C-Flash has to be clicked to configure the FP-30 unit to use these settings. Note that these settings will come to effect only after the **[Write]** button is clicked.

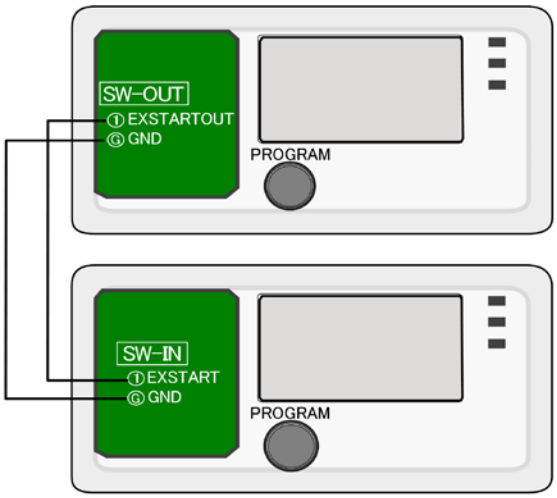


16.2.1 EXSTARTOUT signal

LOW is output on the EXSTARTOUT signal when the **[PROGRAM]** button on the FP-30 unit is pressed. It is in high impedance state otherwise.

When two or more FP-30 units are used, the EXSTARTOUT signal can be connected to the EXSTART signal. When the **[PROGRAM]** button on the first FP-30 unit is pressed, subsequent FP-30 units will also begin the write process. **In this way multiple units can be controlled with a single button press.**

EXSTARTOUT signal is always output and there are no settings on C-Flash to disable it.

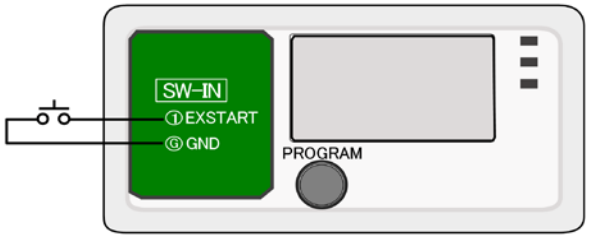


16.2.2 EXSTART signal

EXSTART signal can be used instead of the **[PROGRAM]** button on the FP-30 unit to begin the write operation.

As explained before, multiple FP-30 units can be controlled with a single button press by connecting the EXSTARTOUT signal of one unit to the EXSTART signal of another.

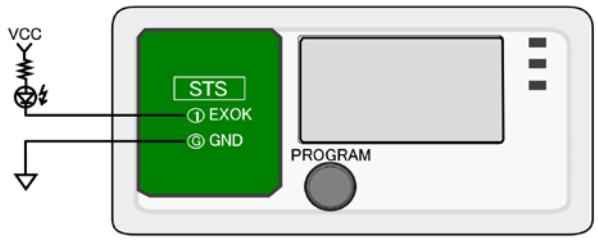
To use this signal, choose **[Enabled]** under **[EXSTART - External Write start signal (input)] group** on the **[External Input/Output settings tab]** on the Detailed settings dialog.



When EXSTART signal is enabled, write operation is started when a low level is detected on this line. During write operation, EXSTART is ignored.

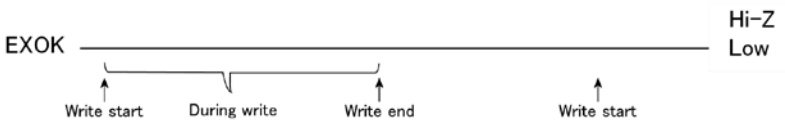
16.2.3 EXOK signal

The status of write operation can be determined using EXOK signal. There are 3 patterns that can be selected from under **[EXOK - External OK signal (output)] group** on the **[External Input/Output settings tab]** on the Detailed settings dialog.

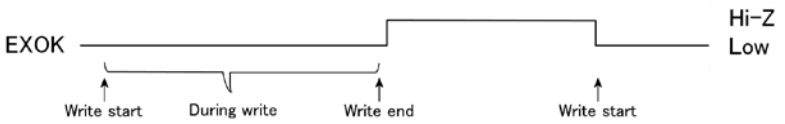


① Low on success, Hi-Z on fail

- **On success**

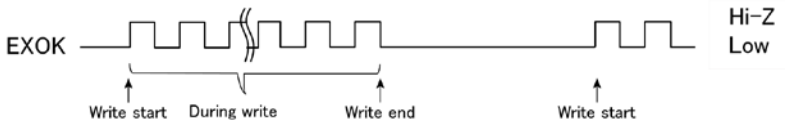


- **On fail**

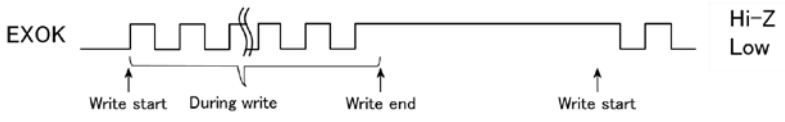


② Pulse output during write, Low on success, Hi-Z on fail

- **On success**

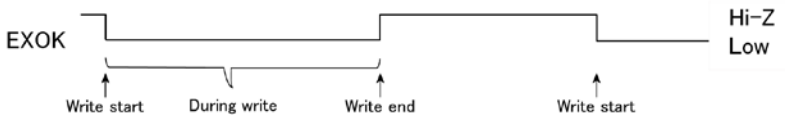


- **On fail**



③ Low during write, Hi-Z after write

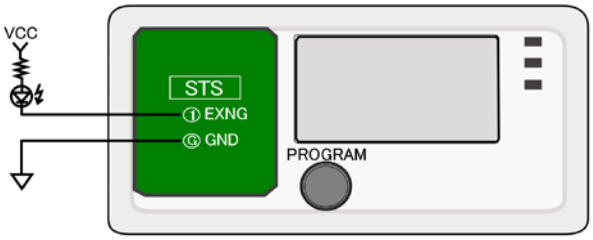
When the write process is in progress, Low is output on EXOK. After write terminates a Hi-Z is output irrespective of whether the write operation succeeds or fails.



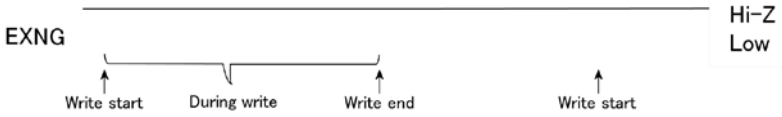
16.2.4 EXNG signal

Success or failure of write operation can be determined using this signal. A low is output during write operation and write success, and high on failure.

To use this signal, choose **[Enabled(Hi-Z on success, Low on fail)]** under **[EXNG - External result signal (output)] group** on the **[External Input/Output settings tab]** on the Detailed settings dialog.



- **On success**



- **On fail**