PALMiCE3

JTAG emulator
PALMiCE3 SH

PALMiCE3 SH is a JTAG emulator that incorporates on-chip debugging function in SuperH family core. HUDI140, the standard model, and AUD360, the model of high-performance edition that supports AUD branch tracing, are available. For both models, the Vbus, which requires no power supply, is supported in PALMiCE3 as the feature was well received in PALMiCE2, and furthermore, it has been materialized to more compact and lighter body. Performance measurement feature and tracing feature have been enhanced even further. As for the debugger, it surely incorporates CSIDE, which provides a user-friendly debugging environment. CSIDE supports not only high-level language debugging of a range of C languages but also fully prepared for the debugging of a range of RTOSs, embedded Linux, and multi-core CPUs. Support for SH7055 Series and H8SX family are also available with optional CSIDE.

*** : HUDI140 model sales has ended.**

- **Supports USB2.0(High-speed), allowing high-speed processing**
- **Has a palm-sized, compact body, but requires no power supply with Vbus support**
- **External/On-chip flash memory downloading capability**
- **Supports high-speed downloading at 1MB/S or higher rate**
- **Simulated I/O feature**
- **Transition display of function (CPU tracing)**
- **Module measurement feature (CPU tracing)**
- **Undo Trace into feature**
- **Capable to provide dual-core support**
- **CPU break feature**
- **Trace-back feature (Optional)**
- **AUD coverage feature (Optional)**
- **Supports SH7055 Series and H8SX family (Optional)**
- **Supports debugging of a range of RTOSs (Optional)**

Main Specifications

		AUD360 model		HUDI140 model
		with AUD probe support	with Mictor probe support	
Supported CPUs	SH-2	SH7047F, SH7083F, SH7084F, SH7085F, SH7086F, SH7124F *3, SH7125F *3, SH7144F, SH7145F, SH7146F, SH7147F *3, SH7149F, SH7606, SH7618, SH7618A, SH7619		
	SH2-DSP	SH7615, SH7616		
	SH-2A	SH7206, SH7211F, SH7243F, SH7285F, SH7286F		
	SH2A-FPU	SH7201, SH7203, SH7261, SH7262, SH7263, SH7264, SH7670, SH7671, SH7672, SH7673		
	SH2A-DUAL	SH7205, SH7265		
	SH-3	SH7705, SH7706, SH7709S		
	SH3-DSP	SH7290(SH-Mobile1), SH7294(SH-MobileJ), SH7300(SH-MobileV), SH7710, SH7712, SH7713, SH7720, SH7721, SH7727, SH7729, SH7729R		
	SH-4	SH7750R, SH7750S, SH7751, SH7751R, SH7760		
	SH-4A	SH7723(SH-MobileR2), SH7730, SH7763, SH7764, SH7770, SH7774, SH7780, SH7781, SH7785		
	SH4AL-DSP	SH7343(SH-Mobile3AS), SH7354(SH-MobileL3V), SH7722(SH-MobileR)		
Target I/F	Voltage	Output : 1.2V - 3.6V (Follows target) or fixed to 3.3V Input : 5V-torelant		1.8V – 5.5V (Follows target) or fixed to 3.3V Note, for 5V-spec CPUs,output level will be min. 4.2V - max. 4.7V.
	Voltage measurement	Measures by sampling and shows the results with accuracy of 50mV and precision showing 2 decimal places.		
	Connector *1	36-pin MDR connector, 43cm probe	38-pin Mictor connector, 43cm probe	14-pin MIL connector, 20cm cable
H-UDI clock		Can be set freely in 0.5MHz increments between 1MHz and 20MHz.		
Transition display of function *2		Presents transition of executed functions as a graph.		
Module measurement feature *2		Indicates function execution time.		
Trace-back feature (Optional) *2		Allows to analyze the information captured into trace memory and implement pseudo execution and back step execution.		
Simulated I/O feature *2		Allows to execute standard input and output function on the target against the host.		
Undo Trace into feature *2		Feature to virtually go back in Trace into execution (Single-step execution)		
AUD coverage feature (Optional) *2		Feature to show the rate of execution for the specified range based on the results of captured AUD trace data. (C0/C1 coverage)		
Register, memory, I/O operation		Supports referencing/editing of register, memory, and I/O and downloading to memory during break. For SH-2A and SH-4A, it supports referencing/editing of register, memory, and I/O even during execution of the user program.		
Flash memory support	On-chip flash memory:	Supports software break settings, ordinary memory rewriting, and also security feature in addition to downloading.		
	External flash memory:	Supports software break settings and ordinary memory rewriting feature in addition to downloading.		
Software break feature		Supports up to 256 points with instruction replacement method.		
Execution time measurement		Measures execution time of the user program (64-bit counter, measurement unit=50nS)		
Debugger included as standard		CSIDE for PALMiCE3 SH-E / CSIDE for PALMiCE3 SH-A-E		
General specifications	Power specification	DC+5V 350mA (Vbus support for USB)		DC+5V 250mA (Vbus support for USB)
	Outside dimensions	95mm(W) ×70mm (D) ×21mm (H)		
	Host I/F	USB mini-B connector		
	Operating environment: Host computer	The computers running on the supported OSs		
	Operating environment: CD drive	Required at the time of installation		
	Operating environment: USB	USB2.0		
	Operating environment: OS	Windows Vista 32-bit version / Windows 7 32-bit version, 64-bit version / Windows 8 32-bit version, 64-bit version		
Product composition contents		PALMiCE3 AUD360 model main unit set / 2m USB cable / dedicated debugger (CD-ROM)		PALMiCE3 HUDI140 model main unit set / 2m USB cable / dedicated debugger (CD-ROM)
Support System		Available		

*1 : Applicable connectors for SH7785 are 38-pin Mictor connector and 14-pin MIL connector. For AUD360 model, P3-SH-PRB-MIC38-MIC38, (optional) target probe, is required.
*2 : Depending on the CPU and model of PALMiCE3, the state of support provision differs. For details, see "Functional Specifications by CPU" page in this document.
*3 : Only supported by ICE-ADP, an optional product.

Functional Specifications by CPU (1/2)

SH-2 / SH2-DSP / SH-2A / SH2A-FPU / SH2A-DUAL

CPU core			SH-2					SH2-DSP	SH-2A			SH2A-FPU/SH2A-DUAL				
Supported CPUs			SH7606 SH7618 SH7618A SH7619	SH7047 SH7144F SH7145F	SH7147F SH7124F SH7125F *5	SH7146F SH7149F SH7083F SH7084F SH7085F SH7086F *5	*6 *7	SH7615 SH7616	SH7243F	SH7211F SH7285F SH7286F	SH7206	SH7201 SH7261	SH7262 SH7264	SH7203 SH7263	SH7205 SH7265	SH7670 SH7671 SH7672 SH7673
CPU break			2 points with UBC (1 of which can be specified by data or pass count)	4 points with UBC (4 of which can be specified by data, or 1 of which can be specified by pass count)	10 points *3		4 points	4 points with UBC (2 of which can be specified by data or pass count)	10 points *3							
CPU tracing feature	H-UDI trace	Number of branches	6	-----	1024		8	4	-----	1024	-----	256		1024		256
		Contents *1	Branching source/destination	-----	Branching source/destination/Data, *4 /Time stamp.		Branching source/de stination	Branching source/destination	-----	Branching source/destination/Data *4 /Time stamp.	-----	Branching source/destination/Data*4 /Time stamp.				
	AUD trace	Number of tracing	-----	512K cycle (with 28-bit / 32-bit time stamp)			-----	-----	512K cycle (with 28-bit time stamp)							-----
		Mode		Prioritize execution / Prioritize tracing					Prioritize execution / Prioritize tracing							
		Clock		Output at 1/2 of CPU clock(Fixed)	Option to choose from 1/1, 1/2, 1/4, 1/8 of CPU clock				Option to choose from 1/1, 1/2, 1/4, 1/8 of CPU clock (For SH7203/63, 1/1 cannot be selected.)							
					40MHz max.	20MHz max.			40MHz max.	50MHz max.						
		Contents *1		Branching destination only/Time stamp.	Branching source/destination/Data/Time stamp. For data access, bus option can be specified.				Branching source/destination/Data/Time stamp. For data access, bus option can be specified.							
Real-time stealing feature *2		*8	-----	△ (RAM monitor)	○ (H-UDI read/write)			-----	○ (H-UDI read/write)							
Transition display of function			-----		○			-----	△	○	△	○				
Module measurement feature			-----		○		-----	-----	△	○	△	○				
Trace-back feature			-----		△		-----	-----	△	○	△	○				
Simulated I/O feature			-----					-----	○					-----		○
AUD coverage feature			-----		△(C0 only)		-----	-----	△(C0/C1)			-----				
Undo Trace into feature			○													

*1: At the time of display, besides the Contents, instructions between branches also will be supplemented (except for the case with branch destination only).
*2: The feature allows referencing /editing of target memory, I/O, and on-chip memory in CPU without even a temporary break during user program execution. It is suitable for target debugging pursuing real-timeliness. RAM monitor feature by AUD(which cannot be used in parallel with branch tracing feature) and H-UDI read/write feature by H-UDI are available.
*3: Instruction (before/after execution option)/Operand address + data: 2 points can be specified.
Instruction (before/after execution option): 1point can be specified.
Instruction (before execution only): 6 points can be specified.
*4: By switching trace targeted buses, access information such as Write/Fetch/DMA also can be acquired.
*5: EVA chip (CPU implemented in ICE-ADP, the optional product)
*6: Debug chip (F-ZTAT version supporting full functions) : R5E7083/R5E7084/R5E7085/R5E7086/R5E7149
*7: Mass-production CPU (Normal F-ZTAT version) : R5F7083/R5F7084/R5F7085/R5F7086/R5F7146

*8: Supporting models
○: Supported by both AUD360 and HUDI140 models
△: Supported by AUD360 model only.
-----: Not supported

Functional Specifications by CPU (2/2)

SH-3 / SH-3DSP / SH4AL-DSP / SH-4A / SH-4

CPU core			SH-3		SH3-DSP			SH4AL-DSP	SH-4A	SH-4	
Supported CPUs			SH7706 SH7709S	SH7705	SH7710 SH7712 SH7713 SH7720 SH7721	SH7727 SH7729 SH7729R	SH7290 (SH-Mobile1) SH7294 (SH-MobileJ) SH7300 (SH-MobileV)	SH7343 (SH-Mobile3AS) SH7354 (SH-MobileL3V) SH7722 (SH-MobileR)	SH7723 (SH-MobileR2) SH7730 SH7763 SH7764 SH7770 SH7774 SH7780 SH7781 SH7785	SH7751 SH7751R SH7760	SH7750S SH7750R
CPU break			Address, data, and status can be specified. Sequential conditions can be specified.								
			2 points with UBC (1 of which can be specified by data or pass count)					11 points *3		4 points (1 of which can be specified by data or pass count)	
CPU tracing feature	H-UDI trace	Number of branches	6					8 (Allows trace data output to the user memory))		6/36	
		Contents *1	Branching source/destination					Branching source/destination/Data/Time stamp. *4		Branching source/destination	
	AUD trace	Number of tracing	512K cycle(with 28-bit / 32-bit time stamp)								
		Mode	Prioritize execution / Prioritize tracing								
		Clock	Option to choose from 80/40/20/10MHz (within a range higher than 1/4 of CPU clock but lower than CPU clock)	Option to choose from 1/1, 1/2, 1/4, 1/8 of CPU clock 80MHz max.	Option to choose from 80/40/20/10MHz (within a range higher than 1/4 of CPU clock but lower than CPU clock)			Option to choose from 1/1, 1/2, 1/4, 1/8 of CPU clock 80MHz max.			-----
		Contents *1	Branching source/destination/Time stamp.	Branching source/destination/Data/Time stamp. For data access, bus option can be specified.	Branching source/destination/Time stamp.			Branching source/destination/Data/Time stamp. For data access, bus option can be specified.			
Real-time stealing feature *2		*5	-----					○ (H-UDI read/write)		-----	
Transition display of function			-----	○	-----			○		○	
Module measurement feature			-----					△		-----	
Trace-back feature			-----	△	-----			○		△	-----
Simulated I/O feature			-----					○		-----	
AUD coverage feature			-----	△(C0 only)	-----			△(C0/C1)		△(C0 only)	-----
Undo Trace into feature			○								

*1: At the time of display, besides the Contents, instructions between branches also will be supplemented (except for the case with branch destination only).

*2: The feature allows referencing /editing of target memory, I/O, and on-chip memory in CPU without even a temporary break during user program execution. It is suitable for target debugging pursuing real-timeliness. RAM monitor feature by AUD(which cannot be used in parallel with branch tracing feature) and H-UDI read/write feature by H-UDI are available.

*3: CPU: 8 points can be specified (Instruction only: 2 points; Instruction/Operand address: 2 points; Instruction/Operand address + data: 2 points; Access break within the memory range you specified: 2 points). SuperHyway bus: 2 points can be specified (by data access). Other: 1 point (Break upon execution of LDTLB instruction).

*4: Available only when outputting trace data to the user memory.

*5: Supporting models
○: Supported by both AUD360 and HUDI140 models
△: Supported by AUD360 model only.
-----: Not supported

Supported languages and supported RTOSs

Supported CPU core		SH-2/SH2-DSP/SH-2ASH2A-FPU/SH2A-DUAL	SH-3/SH3-DSP	SH4AL-DSP	SH-4	SH-4A
Supported C compiler	Renesas C	○				
	GNU C	-----	○			
	GreenHills C	○				
Supported RTOS (Optional)	HI-OS	HI7400, HI7000/4	HI7700, HI7700/4	HI7700/4	HI7750, HI7750/4	
	uC3/Standard	○				
	NORTi	○				
Embedded Linux support (Optional) *1	MontaVista Linux	-----			○	-----
	SuperH.org Linux Ver.2.6.10	-----		○	-----	
	Lineo Linux Ver2.6	-----			○	-----

* : For details on supported CPUs, versions, etc. please contact us.
* : Requires optional debug libraries dedicated to each RTOSs and Linux.
*1 :Supports debugging of, including, but not limited to, kernel, loadable module, and application.

Optional CSIDE

Product name	Description
CSIDE for PALMiCE3 H8S-E	Optional CSIDE for debugging of H8S/H8SX family CPUs.
CSIDE for PALMiCE3 SH7055-E	Optional CSIDE for debugging of SH7055 series CPUs.
CSIDE for PALMiCE3 V850-E	Optional CSIDE for debugging of V850 CPUs.

* : As for the individual CPU support, look it up in our website at http://www.computex.co.jp/asp/cpu/cpu.asp or contact our Sales Department.
* : Together with optional CSIDE, you will need to purchase the respective conversion adapter, etc. that will go in combination with PALMiCE3 main unit. For details, contact our Sales Department.

Other optional products

Product name	Description
ADP-SH-MIL14-MDR36-E	Adapter for conversion from 14-pin MIL connector into 36-pin MDR connector.
ADP-SH-MIL14-MIC38-E	Adapter for conversion from 14-pin MIL connector into 38-pin Mictor connector.
ADP-SH-MDR36-MIL14-E	Adapter for conversion from 36-pin MDR connector into 14-pin MIL connector.
ADP-SH-MIC38-MIL14-E	Adapter for conversion from 38-pin Mictor connector into 14-pin MIL connector.
P3-SH-PRB-MIC38-MIC38-E	Probe that allows direct connection to 38-pin Mictor connector on the target system.
P3-SH-PRB-MIC38-MDR36-E	Probe that allows direct connection to 36-pin MDR connector on the target system.
ICE-ADP *1	CPU in-circuit adapter unit with dedicated EVA chip.

*1 : Specifically for AUD360 model use.
For other details, refer to the Product Summary of ICE-ADP.

Computex

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