



JTAG emulator PALMiCE3 H8S



PALMiCE3 H8S is a JTAG emulator that incorporates on-chip debugging function in H8S and H8SX family cores. It supports USB2.0 (High-speed) as the host interface. Yet, the Vbus, which requires no power supply, is also supported in PALMiCE3 as the feature was well received in PALMiCE2. PALMiCE3 has a palm-sized, light and compact body, providing excellent portability to support you with debugging. As for the debugger, it surely incorporates CSIDE, which provides a user-friendly debugging environment. CSIDE supports not only high-level language debugging of a range of C languages but also fully prepared for the debugging of a range of RTOSs with optional debug libraries. Support for SuperH family is also available with optional CSIDE.

- Supports USB2.0(High-speed), allowing high-speed processing
- A palm-sized, compact body
- Flash memory debugging feature
- Branch tracing feature, CPU break feature
- Requires no power supply with Vbus support
- Undo Trace into feature
- Supports SuperH family (Optional)
- Supports debugging of a range of RTOSs (Optional)

Main Specifications

Supported CPU	H8S *1	H8S/2166F, H8S/2167F, H8S/2168F, H8S/2211F, H8S/2211UF, H8S/2212F, H8S/2212UF, H8S/2215RF, H8S/2215RUF, H8S/2215TF, H8S/2215TUF, H8S/2218F, H8S/2218UF, H8S/2319EF, H8S/2329EF, H8S/2339EF, H8S/2360F, H8S/2361F, H8S/2362F, H8S/2364F, H8S/2367F, H8S/2368F, H8S/2370F, H8S/2370RF, H8S/2371F, H8S/2371RF, H8S/2372F, H8S/2372RF, H8S/2374F, H8S/2374RF, H8S/2377F, H8S/2377RF, H8S/2378F, H8S/2378BF, H8S/2378RF, H8S/2462F	
	H8SX *1	H8SX/1525F, H8SX/1527F, H8SX/1527RF, H8SX/1543F, H8SX/1544F, H8SX/1582F, H8SX/1622F, H8SX/1632F, H8SX/1634F, H8SX/1638F, H8SX/1642F, H8SX/1644F, H8SX/1648F, H8SX/1651, H8SX/1653F, H8SX/1653RF, H8SX/1654F, H8SX/1654RF, H8SX/1658RF, H8SX/1662F, H8SX/1663F, H8SX/1663RF, H8SX/1664F, H8SX/1664RF, H8SX/1665F, H8SX/1668RF	
Target I/F	Voltage	1.65V-5.5V (Follows target).	
	Voltage measurement	Measures by sampling and shows the results with accuracy of 50mV and precision showing 2 decimal places.	
	Connector	14-pin MIL connector, 20cm cable	
H-UDI clock		Can be set freely in 0.5MHz increments between 0.5MHz and 20MHz.	
Register, memory, I/O operation		Supports referencing/editing of register, memory, and I/O and downloading to memory during break.	
Flash memory support	On-chip flash memory:	Supports software break settings and ordinary memory rewriting feature in addition to downloading. Also supports security feature.	
	External flash memory:	Supports software break settings and ordinary memory rewriting feature in addition to downloading. Also, new device support can be added easily by using CSIDE.	
Software break feature		Supports up to 256 points with instruction replacement method.	
CPU break feature *2		Feature in CPU to break at the set bus condition.	
Branch tracing feature *2		Feature to acquire branching information right before the break.	
Execution time measurement		Measures execution time of the user program (64-bit counter, measurement unit=50nS)	
Simulated I/O feature *2		Allows execution of the functions for standard input and output on the target system against the host.	
Undo Trace into feature *2		Feature to virtually go back in Trace into execution (Single-step execution)	
Debugger included as standard		CSIDE for PALMiCE3 H8S-E	
General specifications	Power specification	DC+5V 250mA (Vbus support for USB)	
	Outside dimensions	95mm(W) x70mm (D) x21mm (H)	
	Host I/F	USB mini-B connector	
	Operating environment	Host computer	The computers running on the supported OSs
		CD drive	Required at the time of installation
		USB	USB2.0
		OS	Windows Vista 32-bit version / Windows 7 32-bit version, 64-bit version / Windows 8 32-bit version, 64-bit version
Product composition contents		PALMiCE3 HUDI141 model main unit *3 / H-UDI cable (specifically for PALMiCE3) / 2m USB cable / dedicated debugger (CD-ROM)	
Support System		Available	

*1: In CPUs other than H8S/2300 series and H8SX/1651, expansion mode for disabling on-chip ROM will not work.

*2: Depending on the CPU, the state of support provision differs. For details, see "Functional Specifications by CPU" page in this document.

*3: The HUDI140 model (old model) and the HUDI141 model have the same software specifications.

Functional Specifications by CPU

Supported CPU		H8S	H8SX
CPU break feature		Address, data, and CPU status can be specified.	Address, data, CPU status, and bus cycle can be specified. Sequential break using 2-4 points can be specified.
		2 points	4 points (1 of which can be specified by data or pass count)
Branch tracing feature	Maximum number of branch captures	4 branches	8 branches
	Shows:	Branching source only	Branching source/destination, and supplementation between branches
DTC parallel transfer feature *1		—	○
Simulated I/O feature *2		—	○
Undo Trace into feature		○	—

*1: The feature allows memory access without break during user program execution.

*2: The feature is implemented by DTC parallel transfer feature incorporated.

Supported languages and supported RTOSs

Supported CPU		H8S	H8SX
Supported C compiler	Renesas C	○	○
	HI-OS	HI2000/3	—
Supported RTOS *1 (Optional)	NORTi	○	○

*: For details on supported CPUs, versions, etc. please contact us.

*1: Requires optional debug libraries dedicated to each RTOSs.

Optional CSIDE

Product name	Description
CSIDE for PALMiCE3 SH-E	Optional CSIDE for debugging of SuperH family CPUs.
CSIDE for PALMiCE3 V850-E	Optional CSIDE for debugging of V850 CPUs.

*: As for the individual CPU support, look it up in our website at <http://www.computex.co.jp/asp/cpu/cpu.asp> or contact our Sales Department.

*: Together with optional CSIDE, you will need to purchase the respective conversion adapter, etc. that will go in combination with PALMiCE3 main unit. For details, contact our Sales Department.



Computex Co., Ltd.
<http://www.computex.co.jp/eg/>

<Send inquiries to: >

Head Office Tairanbo Bldg.,
 4-432-13 Gojobashi-Higashi, Higashiyama-ku, KYOTO 6050846 Japan
 E-mail: sales@computex.co.jp

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