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# Technical Information

## ROMiCEmini 80-related Target Interface

Oct. 31, 2008  
First Edition

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**Document change history**

First Editon	Oct. 31, 2008	Initial edition
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## Z80 series

Applicable Product	ROMiCEmini 80
Style of connection	RCN connector connection style or ROM socket connection style

### 1 RCN connector connection style

RCN connector connection style is the connection style which uses the dedicated RCN connector instead of ROM socket in connection. Being the size of connector small, it has advantages in that the space it occupies is minimal, the connection is simple, ...etc. In addition, while the size of emulation memory that can be used in ROM socket connection is determined by the number of addresses connected to ROM socket, in RCN connector connection style, the emulation memory installed on ROMiCEmini can be fully used. Prepare RCN connector at the stage of designing the target board.

For RCN connector connection style, the following 2 I/F specifications are available.

Choose the I/F specification suitable for your use environment.

- **RCN I/F (Standard) specification**

The specification for the time when you use emulation memory within 2MBytes.  
(See "1.1 RCN I/F (Standard) specification")

- **RCN Rev2 I/F (Full-size memory emulation) specification**

The specification for the time when using the emulation memory installed on ROMiCEmini main unit in full size. By the I/F specification, the size varies by the main unit model; in the case of 16M161 model, up to 4MBytes, and in the case of 16M321 model, up to 8MBytes can be used.  
(See "1.2 RCN Rev2 I/F (Full-size memory emulation) specification")

#### 1.1 RCN I/F (Standard) specification

The I/F specification for the time when you use emulation memory within 2MBytes.

Connect the CPU signals or equivalent under Name of signals to be connected.

**Dedicated RCN connector signal table**

No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected
1	TVCC	Output	Power (+1.8V - +5.0V)	2	A0	Output	A0
3	A1	Output	A1	4	A2	Output	A2
5	A3	Output	A3	6	A4	Output	A4
7	A5	Output	A5	8	A6	Output	A6
9	A7	Output	A7	10	A8	Output	A8
11	A9	Output	A9	12	A10	Output	A10
13	A11	Output	A11	14	A12	Output	A12
15	A13	Output	A13	16	A14	Output	A14
17	A15	Output	A15	18	A16	Output	A16
19	A17	Output	A17	20	A18	Output	A18
21	A19	Output	A19	22	A20	Output	A20
23	D0	Input/Output	D0	24	D1	Input/Output	D1
25	D2	Input/Output	D2	26	D3	Input/Output	D3
27	D4	Input/Output	D4	28	D5	Input/Output	D5
29	D6	Input/Output	D6	30	D7	Input/Output	D7
31	D8	Input/Output	N.C.	32	D9	Input/Output	N.C.
33	D10	Input/Output	N.C.	34	D11	Input/Output	N.C.
35	D12	Input/Output	N.C.	36	D13	Input/Output	N.C.
37	D14	Input/Output	N.C.	38	D15	Input/Output	N.C.
39	CE1 <sup>*2</sup>	Output	ROMiCEmini CS signal	40	OE	Output	RD
41	BYTE_CE2	Output	N.C.	42	ST1	Output	N.C.
43	RSTOUT <sup>*3</sup>	Input	RSTOUT signal	44	CS_INH <sup>*4</sup>	Input	CS_INH signal
45	NMIOUT <sup>*3</sup>	Input	NMIOUT signal	46	ST2 <sup>*5</sup>	Output	WR
47	ST3 <sup>*5</sup>	Output	N.C.	48	ST4 <sup>*5</sup>	Output	M1
49	ST5 <sup>*5</sup>	Output	IORQ	50	GND	Output	GND

\* For pins where stated as N.C. in the table, leave signals unconnected.

\*1: Input/output is based on the target system.

\*2: For CE1 pin, connect CS signals of the area for mapping emulation ROM. By ordinary,  $\overline{CS0}$ , the signal of the area with vector address, is to be connected.

\*3: The signals to be connected to  $\overline{RSTOUT}$  and  $\overline{NMIOUT}$  pins are essential. See "1.4 Essential signals" below.

\*4: CS\_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. For details, see "1.5 Other signals" below.

\*5: For ST1 - ST5 pins, connect the signals if you are to use tracing/event feature. For details, see "1.5 Other signals" below.

## 1.2 RCN Rev2 I/F (Full-size memory emulation) specification

The specification for the time when using the emulation memory installed on ROMiCEmini main unit in full size. In the case of this I/F specification, ST14, a status signal for expansion, will not be available. Status signals are for the time when tracing/event features are used.

Connect the CPU signals or equivalent under Name of signals to be connected.

**Dedicated RCN connector signal table**

No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected
1	TVCC	Output	Power (+1.8V - +5.0V)	2	A0	Output	A0
3	A1	Output	A1	4	A2	Output	A2
5	A3	Output	A3	6	A4	Output	A4
7	A5	Output	A5	8	A6	Output	A6
9	A7	Output	A7	10	A8	Output	A8
11	A9	Output	A9	12	A10	Output	A10
13	A11	Output	A11	14	A12	Output	A12
15	A13	Output	A13	16	A14	Output	A14
17	A15	Output	A15	18	A16	Output	A16
19	A17	Output	A17	20	A18	Output	A18
21	A19	Output	A19	22	A20	Output	A20
23	D0	Input/Output	D0	24	D1	Input/Output	D1
25	D2	Input/Output	D2	26	D3	Input/Output	D3
27	D4	Input/Output	D4	28	D5	Input/Output	D5
29	D6	Input/Output	D6	30	D7	Input/Output	D7
31	D8	Input/Output	N.C.	32	D9	Input/Output	N.C.
33	D10	Input/Output	N.C.	34	D11	Input/Output	N.C.
35	D12	Input/Output	N.C.	36	D13	Input/Output	N.C.
37	D14	Input/Output	N.C.	38	D15	Input/Output	N.C.
39	CE1 <sup>*2</sup>	Output	ROMiCEminiCS signal	40	OE	Output	RD
41	BYTE_CE2	Output	N.C.	42	ST1	Output	A21
43	RSTOUT <sup>*3</sup>	Input	RSTOUT signal	44	CS_INH <sup>*4</sup>	Input	CS_INH signal
45	NMIOUT <sup>*3</sup>	Input	NMIOUT signal	46	ST2 <sup>*5</sup>	Output	WR
47	ST3 <sup>*5</sup>	Output	A22	48	ST4 <sup>*5</sup>	Output	M1
49	ST5 <sup>*5</sup>	Output	TORQ	50	GND	Output	GND

• For pins where stated as N.C. in the table, leave signals unconnected.

\*1: Input/output is based on the target system.

\*2: For CE1 pin, connect CS signals of the area for mapping emulation ROM. By ordinary, CS0, the signal of the area with vector address, is to be connected.

\*3: The signals to be connected to RSTOUT and NMIOUT pins are essential. See "1.4 Essential signals" below.

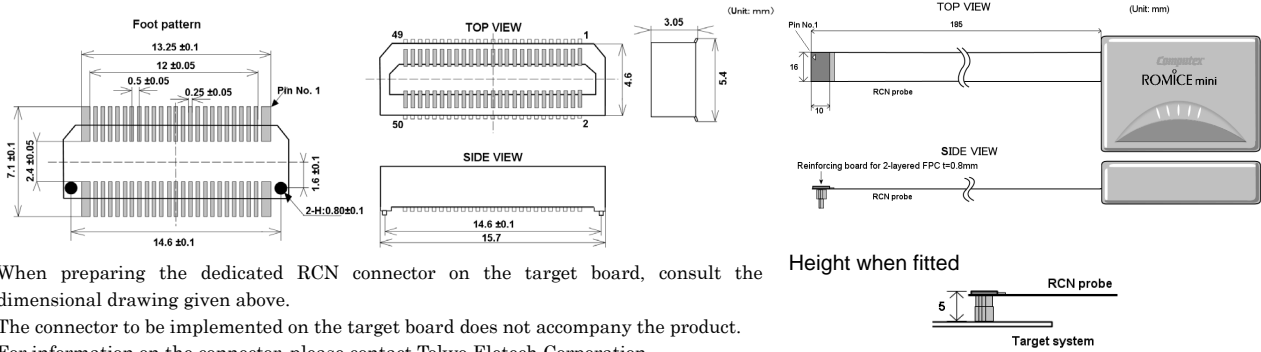
\*4: CS\_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. For details, see "1.5 Other signals" below.

\*5: For ST2 and ST4 - ST5 pins, connect the signals if you are to use tracing/event feature.

For ST1 and ST3 pins, connect address signals for emulation. For details, see "1.5 Other signals" below.

### 1.3 Target Connector Specifications

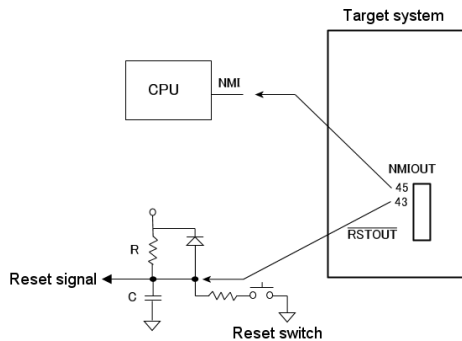
Tokyo Eletech Corporation: SICA2P50S05



When preparing the dedicated RCN connector on the target board, consult the dimensional drawing given above.  
 The connector to be implemented on the target board does not accompany the product.  
 For information on the connector, please contact Tokyo Eletech Corporation.

### 1.4 Essential signals

• RSTOUT, NMIOUT signals



To launch CSIDE and implement Go-Break, RSTOUT and NMIOUT, the output signals from ROMiCEmini, need to be connected.

As shown to the left, connect RSTOUT and NMIOUT pins of RCN connector to the circuit on the target board.

RSTOUT and NMIOUT signals are open-collector output from ROMiCEmini.

Where possible, establish wired OR connection to the RESET circuit on the target board as shown in the drawing.

If the RESET circuit on the target board is of COMS-PUSHPULL, etc., establish the connection via OR circuit.

For the target board using NMI, set up the circuitry that allows NMI signal on the target board to be cut off with jumper pin, etc. when debugging.

### 1.5 Other signals

• Status signals (ST1 - ST5)

**RCN I/F (Standard) specification**

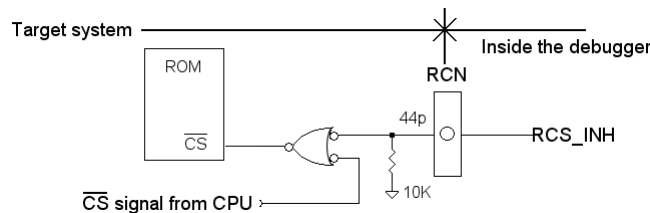
RCN No.	Pin	Connection
42	ST1	The signal of <u>OE</u> pin is to be connected by internal operation.
46	ST2	Connect CPU <u>WR</u> signal. (Standard connection)
47	ST3	N.C. (Standard connection)
48	ST4	Connect CPU <u>M1</u> signal. (Standard connection)
49	ST5	Connect CPU <u>IORQ</u> signal. (Standard connection)

**RCN Rev2 I/F (Full-size memory emulation) specification**

RCN No.	Pin	Connection
42	ST1	Connect CPU <u>A21</u> signal. (For emulation)
46	ST2	Connect CPU <u>WR</u> signal. (Standard connection)
47	ST3	Connect CPU <u>A22</u> signal. (For emulation)
48	ST4	Connect CPU <u>M1</u> signal. (Standard connection)
49	ST5	Connect CPU <u>IORQ</u> signal. (Standard connection)

Connect signals to be traced as status signals when using tracing/event feature. Standard connection is the one that we recommend among the trace connection patterns available. By ordinary, trace data is captured at the signal of OE pin connected to RCN connector as trace clock. In Standard connection, it generates trace clock with combination of patterns from Status signals ST1 – ST5 pins, and then captures trace data at the trace clock. The advantage of using Standard connection is that it allows capturing of trace data at timings of signals other than Read (timings of Read and Write). In Standard connection, the connection patterns given to the left are recommended. For ST1 pin, you do not need to connect a signal because the signal of OE pin is to be connected by ROMiCEmini internal operation. In the case of RCN Rev2 I/F specification, use ST1 and ST3 as address signals for emulation.

• CS\_INH signal

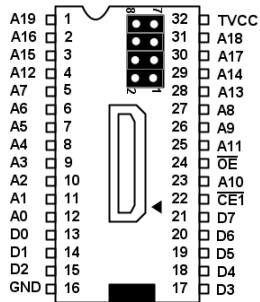


The signal to be output from CS\_INH pin is the output signal for inhibiting access to the ROM on the target board mapped to the same address as emulation ROM area for ROMiCEmini during debugging (while ROMiCEmini is being connected), and always at "H" level. For example, when FLASH ROM directly mounted on the target board and emulation ROM for ROMiCEmini are in the same area, the signal is to be used for inhibiting access to Flash ROM on the target by making OR connections for CS signal and CS\_INH signal of FLASH ROM beforehand so that they do not conflict with each other. The connection is not necessary if the case is not applicable, for example, where the conflict can be avoided by inserting/removing ROM with ROM socket.

## 2 ROM socket connection style

### 2.1 ROM socket signal table

#### •32-pin ROM MAIN socket



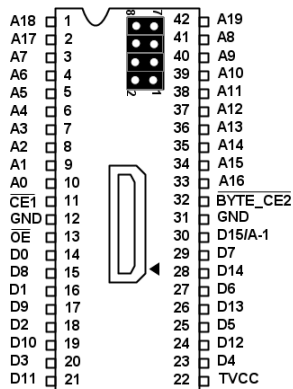
#### Terminal

Pin	Input/ Output <sup>*1</sup>	Description
A <sub>0</sub> - A <sub>19</sub>	Output	Address signals
D <sub>0</sub> - D <sub>7</sub>	Input/ Output	Data signals
$\overline{CE1}$	Output	$\overline{CS}$ signal
$\overline{OE}$	Output	$\overline{RD}$ signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

#### Jumper

No.	Pin	Input/ Output <sup>*1</sup>	Description
1	ST5 <sup>*4</sup>	Output	Status signals
2	ST4 <sup>*4</sup>		
3	ST3 <sup>*4</sup>		
4	ST2 <sup>*4</sup>		
5	NMIOUT <sup>*2</sup>	Input	NMIOUT signal
6	CS_INH <sup>*3</sup>	Input	CS_INH signal
7	$\overline{RSTOUT}$ <sup>*2</sup>	Input	$\overline{RSTOUT}$ signal
8	ST1 <sup>*4</sup>	Output	Status signal

#### •42-pin ROM socket (MASK type)



#### Terminal

Pin	Input/ Output <sup>*1</sup>	Description
A <sub>0</sub> - A <sub>19</sub>	Output	Address signals
D <sub>0</sub> - D <sub>15</sub>	Input/ Output	Data signals
$\overline{CE1}$	Output	$\overline{CS}$ signal
$\overline{BYTE\_CE2}$	Output	$\overline{BYTE/WORD}$
$\overline{OE}$	Output	$\overline{RD}$ signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

#### Jumper

No.	Pin	Input/ Output <sup>*1</sup>	Description
1	ST5 <sup>*4</sup>	Output	Status signals
2	ST4 <sup>*4</sup>		
3	ST3 <sup>*4</sup>		
4	ST2 <sup>*4</sup>		
5	NMIOUT <sup>*2</sup>	Input	NMIOUT signal
6	CS_INH <sup>*3</sup>	Input	CS_INH signal
7	$\overline{RSTOUT}$ <sup>*2</sup>	Input	$\overline{RSTOUT}$ signal
8	ST1 <sup>*4</sup>	Output	Status signal

\*1: Input/output is based on the target system.

\*2: The signals to be connected to  $\overline{RSTOUT}$  and NMIOUT pins are essential. See "2.2 Essential signals" below.

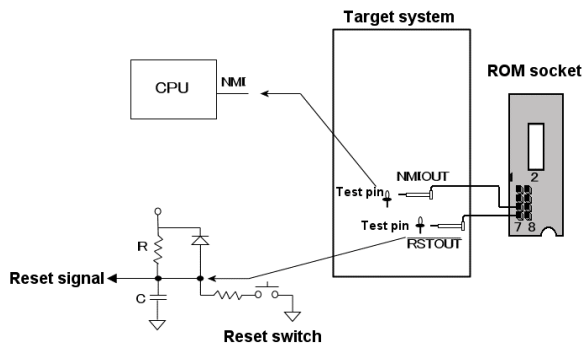
\*3: CS\_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. For details, see "CS\_INH signal" below.

\*4: For ST1 - ST5 pins, connect the signals if you are to use tracing/event feature. For details, see "Status signals" below.

\*5: In 42-pin ROM socket connection,  $\overline{BYTE}$  type connection is accepted.  $\overline{WORD}$  type connection is not supported.

## 2.2 Essential signals

### • $\overline{RSTOUT}$ , NMIOUT signals



To launch CSIDE and implement Go-Break,  $\overline{RSTOUT}$  and NMIOUT, the output signals from ROMiCEmini, need to be connected.

Connect Status 1-8CP probe (200mm) to the jumper pins of ROM socket, and connect the 2 probes to each pin on the target board as shown to the left. Status1-8CP probe has clips at the end. It will be useful if the target board is implemented with the test pin in advance. It will be useful if the target board is implemented with the test pin in advance.

$\overline{RSTOUT}$  and NMIOUT signals are open-collector output from ROMiCEmini.

Where possible, establish wired OR connection to the RESET circuit on the target board as shown in the drawing.

If the RESET circuit on the target board is of COMS-PUSHPULL, etc., establish the connection via OR circuit.

For the target board using NMI, set up the circuitry that allows NMI signal on the target board to be cut off with jumper pin, etc. when debugging.

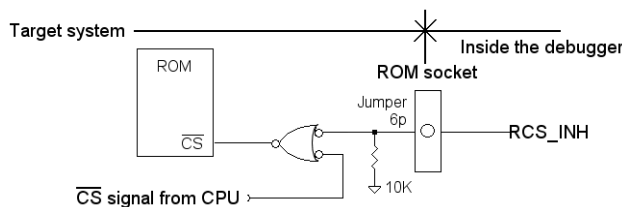
## 2.3 Other signals

### • Status signals (ST1 - ST5)

Pin No.	Signal	Connection
8	ST1	Connect CPU $\overline{RD}$ signal. (Standard connection)
4	ST2	Connect CPU $\overline{WR}$ signal. (Standard connection)
3	ST3	N.C. (Standard connection)
2	ST4	Connect CPU M1 signal. (Standard connection)
1	ST5	Connect CPU $\overline{IORQ}$ signal. (Standard connection)

Connect signals to be traced as status signals when using tracing/event feature. Standard connection is the one that we recommend among the trace connection patterns available. By ordinary, trace data is captured at the signal of  $\overline{OE}$  pin connected to ROM socket as trace clock. In Standard connection, it generates trace clock with combination of patterns from Status signals ST1 – ST5 pins, and then captures trace data at the trace clock. The advantage of using Standard connection is that it allows capturing of trace data at timings of signals other than Read (timings of Read and Write). In Standard connection, the connection patterns given to the left are recommended. For ST1 pin, you do not need to connect a signal because the signal of  $\overline{OE}$  pin is to be connected by ROMiCEmini internal operation.

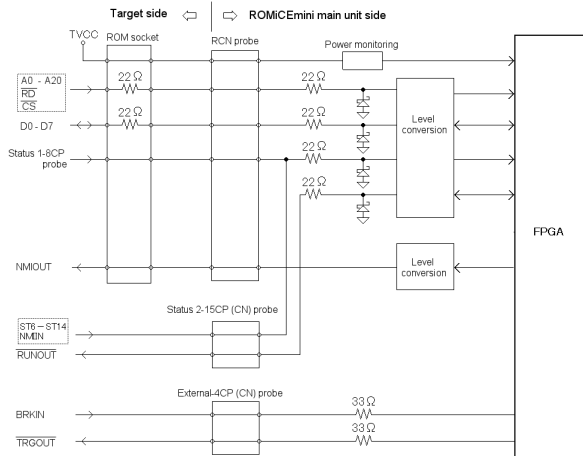
### • CS\_INH signal



The signal to be output from CS\_INH pin is the output signal for inhibiting access to the ROM on the target board mapped to the same address as emulation ROM area for ROMiCEmini during debugging (while ROMiCEmini is being connected), and always at "H" level. For example, when FLASH ROM directly mounted on the target board and emulation ROM for ROMiCEmini are in the same area, the signal is to be used for inhibiting access to Flash ROM on the target by making OR connections for CS signal and CS\_INH signal of FLASH ROM beforehand so that they do not conflict with each other. The connection is not necessary if the case is not applicable, for example, where the conflict can be avoided by inserting/removing ROM with ROM socket.

### 3 Timing specifications

#### 3.1 Target interface block diagram



**Input signal**

All signals except for BRKIN signal support 1.8V - 5V. VIH and VIL are as follows.

Target voltage	VIH	VIL
1.8V - 1.95V	VCCx0.7V and higher	VCCx0.3V and lower
2.3V - 2.7V	1.7V and higher	0.7V and lower
2.7V - 5V	2V and higher	0.8V and lower

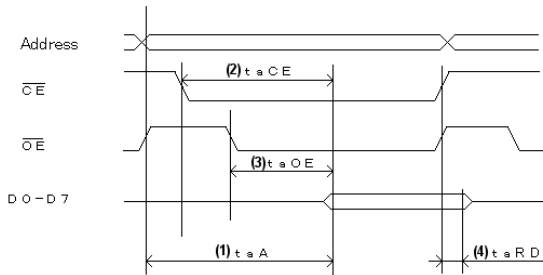
BRKIN signal supports 2.7V - 3.6V. VIH and VIL are as follows.

Target voltage	VIH	VIL
2.7V - 3.6V	2V and higher	0.8V and lower

**Output signal**

D0 - D7 and CS\_INH signals are supported between 1.8V-3.3V. They are output at the electric potential adapted for TVCC, the target power. The electric potential over 3.3V will not be output. NMIOOUT signal is supported between 1.8V-5V. It is output from the buffer that operates by the target power, at electric potential the same as the target. Be aware that for NMIOOUT signal setting, open-collector output is also accepted. RSTOUT signal is an open-collector output from the transistor. TRGOUT signal is output at electric potential of 3.3V.

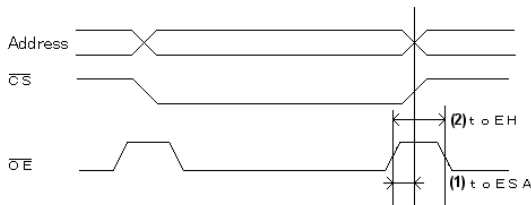
#### 3.2 Emulation ROM access timing



\*: Emulation ROM is an alternate memory incircuited within ROMiCEmini main unit and used as memory to substitute memory on the target board.

Symbol	MIN	MAX	Description
(1) $t_{aA}(\overline{CE}=\overline{OE}=\text{GND})$	-	50ns	Address access time
(2) $t_{aCE}(\overline{OE}=\text{GND})$	-	50ns	$\overline{CE}$ access time
(3) $t_{aOE}(\overline{CE}=\text{GND})$	-	35ns	$\overline{RD}$ access time
(4) $t_{aRD}$	-	25ns	$\overline{RD}$ output disabled time

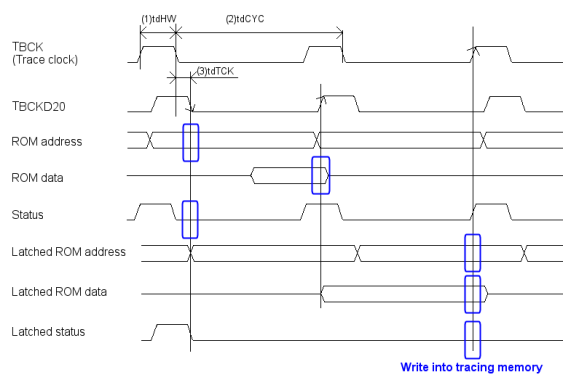
#### 3.3 ROM socket access timing



Specifications	MIN	MAX	Remarks
(1) $t_{oESA}$	0ns	-	-
(2) $t_{oEH}$	10ns	-	It always must be the pulse signal.

\* When ROMiCEmini is to be operated in ROMICE mode, it must satisfy the above timings.

#### 3.4 Trace timing



Specifications	MIN	MAX	Remarks
(1) $t_{dHW}$	10ns	-	-
(2) $t_{dCYC}$	50ns	-	-
(3) $t_{dTCK}$	20ns	-	-

ROMiCEmini latches at the timings of rising and falling of TBCKD20 approx. 20ns delayed from trace clock (TBCK) and writes, at rising edge of trace clock (TBCK), into tracing memory.

The timings for sampling of each signal are in the following 2 patterns:

- Signal to be sampled at rising edge of TBCKD20
  - Data from ROM
- Signals to be sampled at falling edge of TBCKD20
  - Addresses from ROM
  - ST1 - 14

\*: The upper limit value of trace clock is 20MHz. However, it may not be supported in some cases depending on the duty ratio of the clock.

## 4 Specifications of connectors for expansion

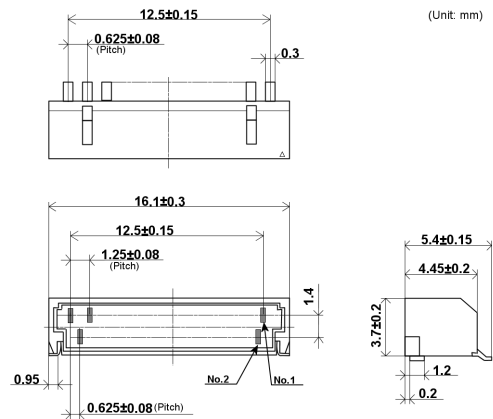
### 4.1 STCN connector

STCN connector is the connector for connecting status signals for tracing/event, and it is to be connected with Status2-15CP probe (Clip type) or Status2-15CN probe (Connector type). Both of the probes are optional.

If you intend to connect Status 2-15CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect Status 2-15CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

For ST6 - ST14 pins, signals are to be connected if you are to use tracing/event feature. Connect the signals to be traced at your own discretion. The connection is not necessary if you do not use it.



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No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected
1	ST6	Output	Status signal of your choice	2	GND	Output	GND
3	ST7			4	GND		
5	ST8			6	GND		
7	ST9			8	GND		
9	ST10			10	GND		
11	ST11			12	GND		
13	ST12			14	GND		
15	ST13			16	GND		
17	ST14 <sup>*4</sup>	18	GND	19	NMIIN	Output	NMIIN <sup>*2</sup>
21	RUNOUT	Input	RUNOUT <sup>*3</sup>	20	GND		

\*1: Input/output is based on the target system.

\*2: For NMIIN pin, connect the NMI signal generated on the target board. Go-Break is implemented at NMIOUT output from ROMiCEmini, but target NMI signal can be used by connecting NMI signal of the target board to NMIIN pin. Set up the circuitry that allows NMI signal on the target board and NMIOUT signal output from ROMiCEmini to be cut off with jumper pin, etc. when debugging. The connection is not necessary if you do not use it.

\*3: RUNOUT signal is a negative logic signal output from ROMiCEmini. It is output at "L" during execution of the user program. If output at "H", it means that the user program is in break. The connection is not necessary if you do not use it.

\*4: In the case of RCN Rev2 I/F specification, leave it as N.C.. ST14 cannot be used.

### 4.2 EXTCN connector

EXTCN connector is the connector for connecting TRGOUT, BRKIN signals, and it is to be connected with External-4CP probe (Clip type) or External-4CN probe (Connector type).

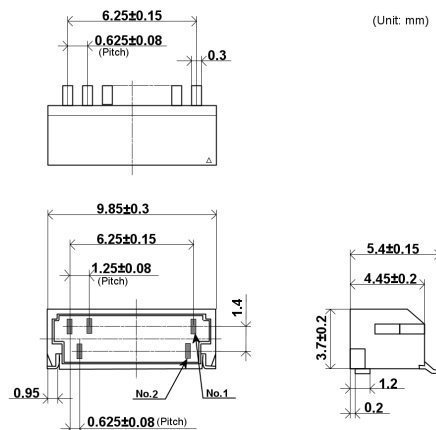
Both of the probes are optional.

If you intend to connect External-4CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect External-4CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

TRGOUT pin outputs TRGOUT signal of 1 pulse (negative logic) from ROMiCEmini if matched with the specified condition during the user program execution. The output voltage is at 3.3V. The connection is not required if you do not intend to use it.

BRKIN pin inputs the signal for external force break from outside. It is to be used when you wish to break the user program by external signal of your choice. The setting can be switched between the edges, rising or falling. The connection is not required if you do not intend to use it.



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No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected
1	TRGOUT	Input	TRGOUT	2	GND	Output	GND
3	N.C.	-	-	4	GND		
5	N.C.	-	-	6	GND		
7	N.C.	-	-	8	GND		
9	BRKIN	Output	BRKIN	10	GND		
11	+5.0V	Input	Power <sup>*</sup>				

\* For pins where stated as N.C. in the table, leave signals unconnected.

\* +5.0V power is supplied from ROMiCEmini main unit. By ordinary, leave it unconnected.

\*1: Input/output is based on the target system.

## Document change history (Z80)

First Editon	Oct. 31,2008	Initial edition (Changed to a new format)
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## ■ LR35501/03(Sharp-made)

Applicable Product	ROMiCEmini 80
Style of connection	RCN connector connection style or ROM socket connection style

### 1 RCN connector connection style

RCN connector connection style is the connection style which uses the dedicated RCN connector instead of ROM socket in connection. Being the size of connector small, it has advantages in that the space it occupies is minimal, the connection is simple, ...etc. In addition, while the size of emulation memory that can be used in ROM socket connection is determined by the number of addresses connected to ROM socket, in RCN connector connection style, the emulation memory installed on ROMiCEmini can be fully used. Prepare RCN connector at the stage of designing the target board.

For RCN connector connection style, the following 2 I/F specifications are available.

Choose the I/F specification suitable for your use environment.

- **RCN I/F (Standard) specification**

The specification for the time when you use emulation memory within 2MBytes.  
(See "1.1 RCN I/F (Standard) specification")

- **RCN Rev2 I/F (Full-size memory emulation) specification**

The specification for the time when using the emulation memory installed on ROMiCEmini main unit in full size. By the I/F specification, the size varies by the main unit model; in the case of 16M161 model, up to 4MBytes, and in the case of 16M321 model, up to 8MBytes can be used.  
(See "1.2 RCN Rev2 I/F (Full-size memory emulation) specification")

#### 1.1 RCN I/F (Standard) specification

The I/F specification for the time when you use emulation memory within 2MBytes.

Connect the CPU signals or equivalent under Name of signals to be connected.

**Dedicated RCN connector signal table**

No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected
1	TVCC	Output	Power (+1.8V - +5.0V)	2	A0	Output	A0
3	A1	Output	A1	4	A2	Output	A2
5	A3	Output	A3	6	A4	Output	A4
7	A5	Output	A5	8	A6	Output	A6
9	A7	Output	A7	10	A8	Output	A8
11	A9	Output	A9	12	A10	Output	A10
13	A11	Output	A11	14	A12	Output	A12
15	A13	Output	A13	16	A14	Output	A14
17	A15	Output	A15	18	A16	Output	A16
19	A17	Output	A17	20	A18	Output	A18
21	A19	Output	A19	22	A20	Output	A20
23	D0	Input/Output	D0	24	D1	Input/Output	D1
25	D2	Input/Output	D2	26	D3	Input/Output	D3
27	D4	Input/Output	D4	28	D5	Input/Output	D5
29	D6	Input/Output	D6	30	D7	Input/Output	D7
31	D8	Input/Output	N.C.	32	D9	Input/Output	N.C.
33	D10	Input/Output	N.C.	34	D11	Input/Output	N.C.
35	D12	Input/Output	N.C.	36	D13	Input/Output	N.C.
37	D14	Input/Output	N.C.	38	D15	Input/Output	N.C.
39	CE1 <sup>*2</sup>	Output	ROMiCEmini CS signal	40	OE	Output	RD
41	BYTE_CE2	Output	N.C.	42	ST1	Output	N.C.
43	RSTOUT <sup>*3</sup>	Input	RSTOUT signal	44	CS_INH <sup>*4</sup>	Input	CS_INH signal
45	NMIOUT <sup>*3</sup>	Input	NMIOUT signal	46	ST2 <sup>*5</sup>	Output	N.C.
47	ST3 <sup>*5</sup>	Output	N.C.	48	ST4 <sup>*5</sup>	Output	N.C.
49	ST5 <sup>*5</sup>	Output	N.C.	50	GND	Output	GND

• For pins where stated as N.C. in the table, leave signals unconnected.

\*1: Input/output is based on the target system.

\*2: For CE1 pin, connect CS signals of the area for mapping emulation ROM. By ordinary, CS0, the signal of the area with vector address, is to be connected.

\*3: The signals to be connected to RSTOUT and NMIOUT pins are essential. See "1.4 Essential signals" below.

\*4: CS\_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. For details, see "1.5 Other signals" below.

\*5: For ST1 - ST5 pins, connect the signals if you are to use tracing/event feature. See "1.5 Other signals" below.

## 1.2 RCN Rev2 I/F (Full-size memory emulation) specification

The specification for the time when using the emulation memory installed on ROMiCEmini main unit in full size. In the case of this I/F specification, ST14, a status signal for expansion, will not be available. Status signals are for the time when tracing/event features are used.

Connect the CPU signals or equivalent under Name of signals to be connected.

**Dedicated RCN connector signal table**

No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin name	Input/Output <sup>*1</sup>	Name of signals to be connected
1	TVCC	Output	Power (+1.8V - +5.0V)	2	A0	Output	A0
3	A1	Output	A1	4	A2	Output	A2
5	A3	Output	A3	6	A4	Output	A4
7	A5	Output	A5	8	A6	Output	A6
9	A7	Output	A7	10	A8	Output	A8
11	A9	Output	A9	12	A10	Output	A10
13	A11	Output	A11	14	A12	Output	A12
15	A13	Output	A13	16	A14	Output	A14
17	A15	Output	A15	18	A16	Output	A16
19	A17	Output	A17	20	A18	Output	A18
21	A19	Output	A19	22	A20	Output	A20
23	D0	Input/Output	D0	24	D1	Input/Output	D1
25	D2	Input/Output	D2	26	D3	Input/Output	D3
27	D4	Input/Output	D4	28	D5	Input/Output	D5
29	D6	Input/Output	D6	30	D7	Input/Output	D7
31	D8	Input/Output	N.C.	32	D9	Input/Output	N.C.
33	D10	Input/Output	N.C.	34	D11	Input/Output	N.C.
35	D12	Input/Output	N.C.	36	D13	Input/Output	N.C.
37	D14	Input/Output	N.C.	38	D15	Input/Output	N.C.
39	CE1 <sup>*2</sup>	Output	ROMiCEminiCS signal	40	OE	Output	RD
41	BYTE_CE2	Output	N.C.	42	ST1	Output	A21
43	RSTOUT <sup>*3</sup>	Input	RSTOUT signal	44	CS_INH <sup>*4</sup>	Input	CS_INH signal
45	NMIOUT <sup>*3</sup>	Input	NMIOUT signal	46	ST2 <sup>*5</sup>	Output	N.C.
47	ST3 <sup>*5</sup>	Output	A22	48	ST4 <sup>*5</sup>	Output	N.C.
49	ST5 <sup>*5</sup>	Output	N.C.	50	GND	Output	GND

• For pins where stated as N.C. in the table, leave signals unconnected.

\*1: Input/output is based on the target system.

\*2: For CE1 pin, connect CS signals of the area for mapping emulation ROM. By ordinary, CS0, the signal of the area with vector address, is to be connected.

\*3: The signals to be connected to RSTOUT and NMIOUT pins are essential. See "1.4 Essential signals" below.

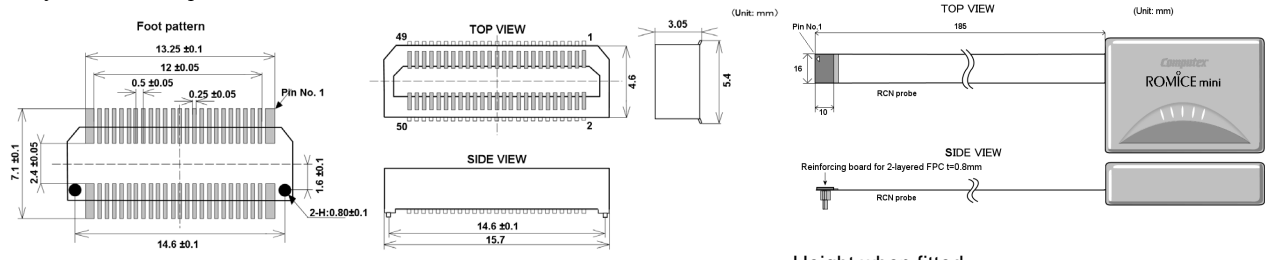
\*4: CS\_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. For details, see "1.5 Other signals" below.

\*5: For ST2 and ST4 - ST5 pins, connect the signals if you are to use tracing/event feature.

For ST1 and ST3 pins, connect address signals for emulation. For details, see "1.5 Other signals" below.

### 1.3 Target Connector Specifications

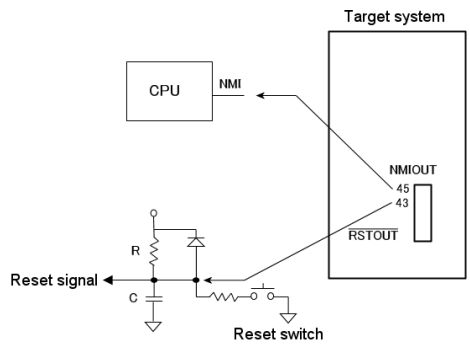
Tokyo Eletech Corporation: SICA2P50S05



When preparing the dedicated RCN connector on the target board, consult the dimensional drawing given above.  
 The connector to be implemented on the target board does not accompany the product.  
 For information on the connector, please contact Tokyo Eletech Corporation.

### 1.4 Essential signals

•  $\overline{RSTOUT}$ , NMIOUT signals



To launch CSIDE and implement Go-Break,  $\overline{RSTOUT}$  and NMIOUT, the output signals from ROMiCEmini, need to be connected.  
 As shown to the left, connect  $\overline{RSTOUT}$  and NMIOUT pins of RCN connector to the circuit on the target board.  
 $\overline{RSTOUT}$  and NMIOUT signals are open-collector output from ROMiCEmini.  
 Where possible, establish wired OR connection to the RESET circuit on the target board as shown in the drawing.  
 If the RESET circuit on the target board is of COMS-PUSHPULL, etc., establish the connection via OR circuit.  
 For the target board using NMI, set up the circuitry that allows NMI signal on the target board to be cut off with jumper pin, etc. when debugging.

### 1.5 Other signals

• Status signals (ST1 - ST5)

**RCN I/F (Standard) specification**

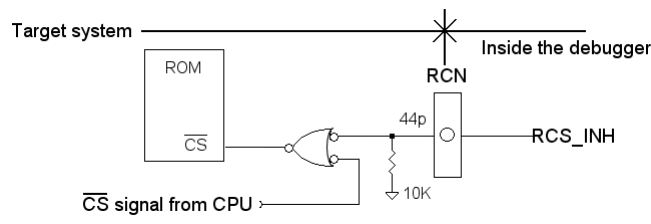
RCN No.	Pin	Connection
42	ST1	The signal of $\overline{OE}$ pin is to be connected by internal operation.
46	ST2	N.C. (Standard connection)
47	ST3	N.C. (Standard connection)
48	ST4	N.C. (Standard connection)
49	ST5	N.C. (Standard connection)

**RCN Rev2 I/F (Full-size memory emulation) specification**

RCN No.	Pin	Connection
42	ST1	Connect CPU A21 signal. (For emulation)
46	ST2	N.C. (Standard connection)
47	ST3	Connect CPU A22 signal. (For emulation)
48	ST4	N.C. (Standard connection)
49	ST5	N.C. (Standard connection)

Connect signals to be traced as status signals when using tracing/event feature. Standard connection is the one that we recommend among the trace connection patterns available. By ordinary, trace data is captured at the signal of  $\overline{OE}$  pin connected to RCN connector as trace clock. In Standard connection, it generates trace clock with combination of patterns from Status signals ST1 – ST5 pins, and then captures trace data at the trace clock. The advantage of using Standard connection is that it allows capturing of trace data at timings of signals other than Read (timings of Read and Write). In Standard connection, the connection patterns given to the left are recommended. For ST1 pin, you do not need to connect a signal because the signal of  $\overline{OE}$  pin is to be connected by ROMiCEmini internal operation.  
 In the case of RCN Rev2 I/F specification, use ST1 and ST3 as address signals for emulation.

• CS\_INH signal

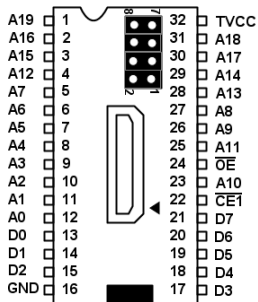


The signal to be output from CS\_INH pin is the output signal for inhibiting access to the ROM on the target board mapped to the same address as emulation ROM area for ROMiCEmini during debugging (while ROMiCEmini is being connected), and always at "H" level. For example, when FLASH ROM directly mounted on the target board and emulation ROM for ROMiCEmini are in the same area, the signal is to be used for inhibiting access to Flash ROM on the target by making OR connections for CS signal and CS\_INH signal of FLASH ROM beforehand so that they do not conflict with each other. The connection is not necessary if the case is not applicable, for example, where the conflict can be avoided by inserting/removing ROM with ROM socket.

## 2 ROM socket connection style

### 2.1 ROM socket signal table

#### •32-pin ROM MAIN socket



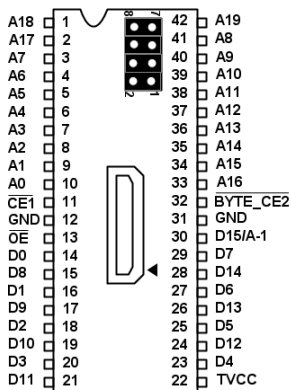
#### Terminal

Pin	Input/ Output <sup>*1</sup>	Description
A <sub>0</sub> - A <sub>19</sub>	Output	Address signals
D <sub>0</sub> - D <sub>7</sub>	Input/ Output	Data signals
$\overline{CE1}$	Output	$\overline{CS}$ signal
$\overline{OE}$	Output	$\overline{RD}$ signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

#### Jumper

No.	Pin	Input/ Output <sup>*1</sup>	Description
1	ST5 <sup>*4</sup>	Output	Status signals
2	ST4 <sup>*4</sup>		
3	ST3 <sup>*4</sup>		
4	ST2 <sup>*4</sup>		
5	NMIOUT <sup>*2</sup>	Input	NMIOUT signal
6	CS_INH <sup>*3</sup>	Input	CS_INH signal
7	RSTOUT <sup>*2</sup>	Input	RSTOUT signal
8	ST1 <sup>*4</sup>	Output	Status signal

#### •42-pin ROM socket (MASK type)



#### Terminal

Pin	Input/ Output <sup>*1</sup>	Description
A <sub>0</sub> - A <sub>19</sub>	Output	Address signals
D <sub>0</sub> - D <sub>15</sub>	Input/ Output	Data signals
$\overline{CE1}$	Output	$\overline{CS}$ signal
BYTE_CE2	Output	$\overline{BYTE}/\overline{WORD}$
$\overline{OE}$	Output	$\overline{RD}$ signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

#### Jumper

No.	Pin	Input/ Output <sup>*1</sup>	Description
1	ST5 <sup>*4</sup>	Output	Status signals
2	ST4 <sup>*4</sup>		
3	ST3 <sup>*4</sup>		
4	ST2 <sup>*4</sup>		
5	NMIOUT <sup>*2</sup>	Input	NMIOUT signal
6	CS_INH <sup>*3</sup>	Input	CS_INH signal
7	RSTOUT <sup>*2</sup>	Input	RSTOUT signal
8	ST1 <sup>*4</sup>	Output	Status signal

\*1: Input/output is based on the target system.

\*2: The signals to be connected to RSTOUT and NMIOUT pins are essential. See "2.2 Essential signals" below.

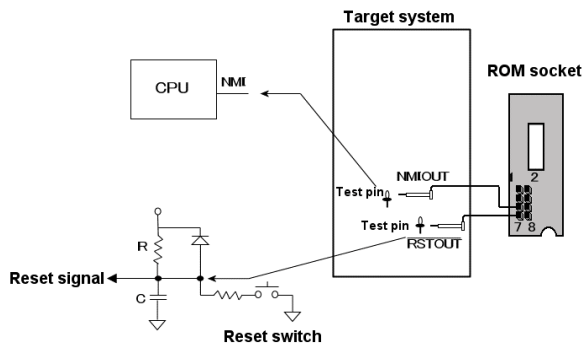
\*3: CS\_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. For details, see "CS\_INH signal" below.

\*4: For ST1 - ST5 pins, connect the signals if you are to use tracing/event feature. For details, see "Status signals" below.

\*5: In 42-pin ROM socket connection, BYTE type connection is accepted. WORD type connection is not supported.

## 2.2 Essential signals

### • $\overline{\text{RSTOUT}}$ , NMIOUT signals



To launch CSIDE and implement Go-Break,  $\overline{\text{RSTOUT}}$  and NMIOUT, the output signals from ROMiCEmini, need to be connected.

Connect Status 1-8CP probe (200mm) to the jumper pins of ROM socket, and connect the 2 probes to each pin on the target board as shown to the left. Status1-8CP probe has clips at the end. It will be useful if the target board is implemented with the test pin in advance. It will be useful if the target board is implemented with the test pin in advance.

$\overline{\text{RSTOUT}}$  and NMIOUT signals are open-collector output from ROMiCEmini.

Where possible, establish wired OR connection to the RESET circuit on the target board as shown in the drawing.

If the RESET circuit on the target board is of COMS-PUSHPULL, etc., establish the connection via OR circuit.

For the target board using NMI, set up the circuitry that allows NMI signal on the target board to be cut off with jumper pin, etc. when debugging.

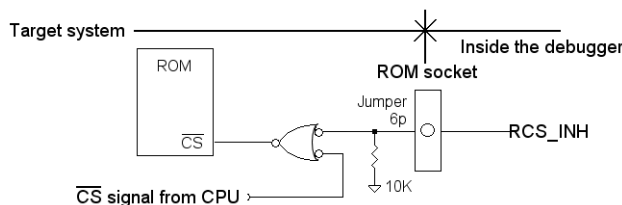
## 2.3 Other signals

### • Status signals (ST1 - ST5)

Pin No.	Signal	Connection
8	ST1	Connect CPU $\overline{\text{RD}}$ signal. (Standard connection)
4	ST2	N.C. (Standard connection)
3	ST3	N.C. (Standard connection)
2	ST4	N.C. (Standard connection)
1	ST5	N.C. (Standard connection)

Connect signals to be traced as status signals when using tracing/event feature. Standard connection is the one that we recommend among the trace connection patterns available. By ordinary, trace data is captured at the signal of  $\overline{\text{OE}}$  pin connected to ROM socket as trace clock. In Standard connection, it generates trace clock with combination of patterns from Status signals ST1 – ST5 pins, and then captures trace data at the trace clock. The advantage of using Standard connection is that it allows capturing of trace data at timings of signals other than Read (timings of Read and Write). In Standard connection, the connection patterns given to the left are recommended. For ST1 pin, you do not need to connect a signal because the signal of  $\overline{\text{OE}}$  pin is to be connected by ROMiCEmini internal operation.

### • CS\_INH signal

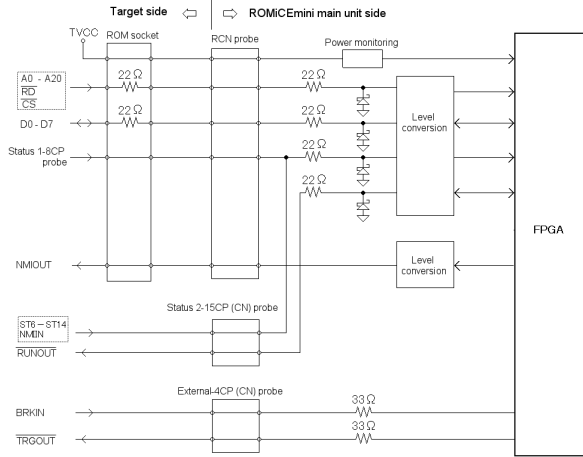


The signal to be output from CS\_INH pin is the output signal for inhibiting access to the ROM on the target board mapped to the same address as emulation ROM area for ROMiCEmini during debugging (while ROMiCEmini is being connected), and always at "H" level. For example, when FLASH ROM directly mounted on the target board and emulation ROM for ROMiCEmini are in the same area, the signal is to be used for inhibiting access to Flash ROM on the target by making OR connections for CS signal and CS\_INH signal of FLASH ROM beforehand so that they do not conflict with each other. The connection is not necessary if the case is not applicable, for example, where the conflict can be avoided by inserting/removing ROM with ROM socket.

The size available in EML varies depending on the number of addresses.

### 3 Timing specifications

#### 3.1 Target interface block diagram



**Input signal**

All signals except for BRKIN signal support 1.8V - 5V. VIH and VIL are as follows.

Target voltage	VIH	VIL
1.8V - 1.95V	VCCx0.7V and higher	VCCx0.3V and lower
2.3V - 2.7V	1.7V and higher	0.7V and lower
2.7V - 5V	2V and higher	0.8V and lower

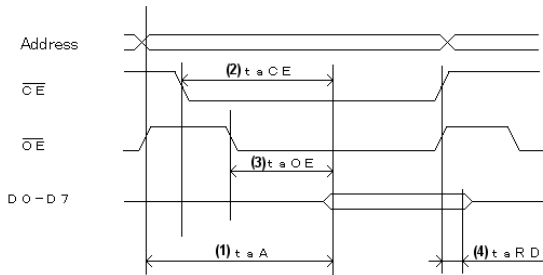
BRKIN signal supports 2.7V - 3.6V. VIH and VIL are as follows.

Target voltage	VIH	VIL
2.7V - 3.6V	2V and higher	0.8V and lower

**Output signal**

D0 - D7 and CS\_INH signals are supported between 1.8V-3.3V. They are output at the electric potential adapted for TVCC, the target power. The electric potential over 3.3V will not be output. NMIOOUT signal is supported between 1.8V-5V. It is output from the buffer that operates by the target power, at electric potential the same as the target. Be aware that for NMIOOUT signal setting, open-collector output is also accepted. RSTOUT signal is an open-collector output from the transistor. TRGOUT signal is output at electric potential of 3.3V.

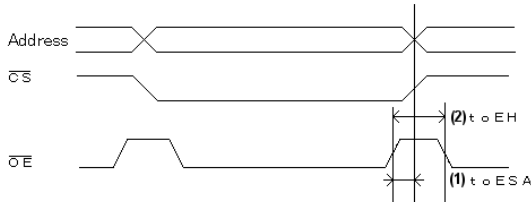
#### 3.2 Emulation ROM access timing



\*: Emulation ROM is an alternate memory incircuited within ROMiCEmini main unit and used as memory to substitute memory on the target board.

Symbol	MIN	MAX	Description
(1) $t_{aA} (CE=OE=GND)$	-	50ns	Address access time
(2) $t_{aCE} (OE=GND)$	-	50ns	$\overline{CE}$ access time
(3) $t_{aOE} (CE=GND)$	-	35ns	$\overline{RD}$ access time
(4) $t_{aRD}$	-	25ns	$\overline{RD}$ output disabled time

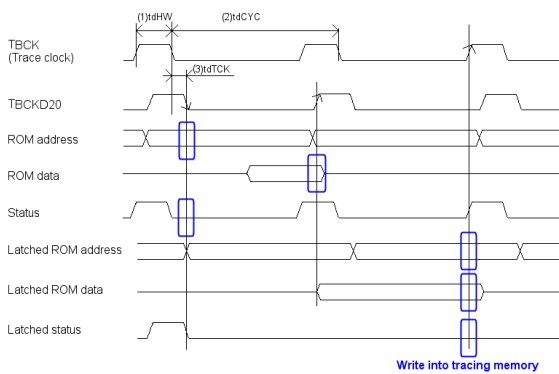
#### 3.3 ROM socket access timing



Specifications	MIN	MAX	Remarks
(1) $t_{oESA}$	0ns	-	-
(2) $t_{oEH}$	10ns	-	It always must be the pulse signal.

\* When ROMiCEmini is to be operated in ROMICE mode, it must satisfy the above timings.

#### 3.4 Trace timing



Specifications	MIN	MAX	Remarks
(1) $t_{dHW}$	10ns	-	-
(2) $t_{dCYC}$	50ns	-	-
(3) $t_{dTCK}$	20ns	-	-

ROMiCEmini latches at the timings of rising and falling of TBCKD20 approx. 20ns delayed from trace clock (TBCK) and writes, at rising edge of trace clock (TBCK), into tracing memory.

The timings for sampling of each signal are in the following 2 patterns:

- Signal to be sampled at rising edge of TBCKD20
  - Data from ROM
  - Addresses from ROM
  - ST1 - 14
- Signals to be sampled at falling edge of TBCKD20
  - Addresses from ROM
  - ST1 - 14

\*: The upper limit value of trace clock is 20MHz. However, it may not be supported in some cases depending on the duty ratio of the clock.

## 4 Specifications of connectors for expansion

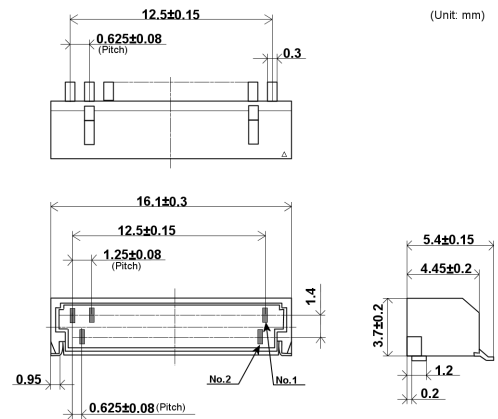
### 4.1 STCN connector

STCN connector is the connector for connecting status signals for tracing/event, and it is to be connected with Status2-15CP probe (Clip type) or Status2-15CN probe (Connector type). Both of the probes are optional.

If you intend to connect Status 2-15CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect Status 2-15CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

For ST6 - ST14 pins, signals are to be connected if you are to use tracing/event feature. Connect the signals to be traced at your own discretion. The connection is not necessary if you do not use it.



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No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected
1	ST6	Output	Status signal of your choice	2	GND	Output	GND
3	ST7			4	GND		
5	ST8			6	GND		
7	ST9			8	GND		
9	ST10			10	GND		
11	ST11			12	GND		
13	ST12			14	GND		
15	ST13			16	GND		
17	ST14 <sup>*4</sup>	18	GND				
19	NMIIN	Output	NMIIN <sup>*2</sup>	20	GND		
21	RUNOUT	Input	RUNOUT <sup>*3</sup>				

\*1: Input/output is based on the target system.

\*2: For NMIIN pin, connect the NMI signal generated on the target board. Go-Break is implemented at NMIOUT output from ROMiCEmini, but target NMI signal can be used by connecting NMI signal of the target board to NMIIN pin. Set up the circuitry that allows NMI signal on the target board and NMIOUT signal output from ROMiCEmini to be cut off with jumper pin, etc. when debugging. The connection is not necessary if you do not use it.

\*3: RUNOUT signal is a negative logic signal output from ROMiCEmini. It is output at "L" during execution of the user program. If output at "H", it means that the user program is in break. The connection is not necessary if you do not use it.

\*4: In the case of RCN Rev2 I/F specification, leave it as N.C.. ST14 cannot be used.

### 4.2 EXTCN connector

EXTCN connector is the connector for connecting TRGOUT, BRKIN signals, and it is to be connected with External-4CP probe (Clip type) or External-4CN probe (Connector type).

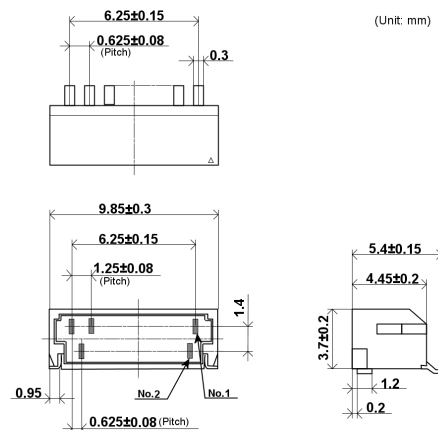
Both of the probes are optional.

If you intend to connect External-4CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect External-4CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

TRGOUT pin outputs TRGOUT signal of 1 pulse (negative logic) from ROMiCEmini if matched with the specified condition during the user program execution. The output voltage is at 3.3V. The connection is not required if you do not intend to use it.

BRKIN pin inputs the signal for external force break from outside. It is to be used when you wish to break the user program by external signal of your choice. The setting can be switched between the edges, rising or falling. The connection is not required if you do not intend to use it.



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No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected	No.	Pin	Input/Output <sup>*1</sup>	Name of signals to be connected
1	TRGOUT	Input	TRGOUT	2	GND	Output	GND
3	N.C.	-	-	4	GND		
5	N.C.	-	-	6	GND		
7	N.C.	-	-	8	GND		
9	BRKIN	Output	BRKIN	10	GND		
11	+5.0V	Input	Power <sup>*</sup>				

\* For pins where stated as N.C. in the table, leave signals unconnected.

\* +5.0V power is supplied from ROMiCEmini main unit. By ordinary, leave it unconnected.

\*1: Input/output is based on the target system.

## Document change history (LR35501/03(Sharp-made))

First Editon	Oct. 31,2008	Initial edition (Changed to a new format)
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