



Target Interface Specifications (ROM socket connection style)

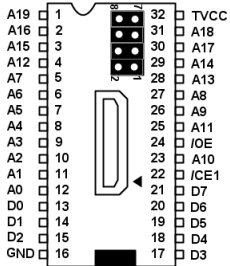
● ROM socket signal table

Input and output are stated from the target board's point of view.

- \*1: The signals to be connected to /RSTOUT and NMIOUT pins are essential. See below.
- \*2: CS\_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. See below for details.

- \*3: For ST1 - ST5 pins, connect the signals if you are to use tracing/event feature. See below for details.
- \*4: Address signals to be connected to ROM socket varies depending on the bus width. In the case of 8-bit bus, start from A0 of CPU in connecting the signals. In the case of 16-bit bus, start from A1 of CPU in connecting the signals.

32-pin ROM MAIN socket



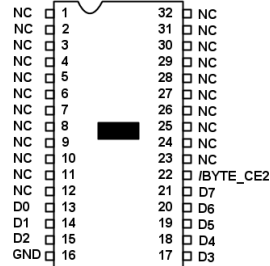
Terminal

Pin	Input/Output	Description
A <sub>0</sub> - A <sub>19</sub>	Output	Address signals
D <sub>0</sub> - D <sub>7</sub>	Input/Output	Data signals
/CE1	Output	/CS signal
/OE	Output	/RD signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

Jumper

No.	Pin	Input/Output	Description
1	ST5 <sup>3</sup>	Output	Status signals
2	ST4 <sup>3</sup>		
3	ST3 <sup>3</sup>		
4	ST2 <sup>3</sup>		
5	NMIOUT <sup>1</sup>	Input	NMIOUT signal
6	CS_INH <sup>2</sup>	Input	CS_INH signal
7	/RSTOUT <sup>1</sup>	Input	/RSTOUT signal
8	ST1 <sup>3</sup>	Output	Status signal

32-pin ROM SUB socket



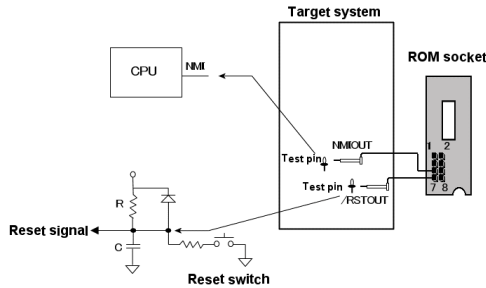
Terminal

Pin	Input/Output	Description
NC*	-	-
D <sub>0</sub> - D <sub>7</sub>	Input/Output	Data signals
/BYTE_CE2	Output	/CS signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

\*Even if signals such as address are connected to NC, it does not matter.

● Essential signals

-/RSTOUT, NMIOUT signals



To launch CSIDE and implement Go-Break, /RSTOUT and NMIOUT, the output signals from ROMiCEmini, need to be connected.

Connect Status 1-8CP probe (200mm) to the jumper pins of ROM socket, and connect the 2 probes to each pin on the target board as shown to the left. Status1-8CP probe has clips at the end. It will be useful if the target board is implemented with the test pin in advance.

/RSTOUT and NMIOUT signals are open-collector output from ROMiCEmini.

Where possible, establish wired OR connection to the RESET circuit on the target board as shown in the drawing. If the RESET circuit on the target board is of COMS-PUSHPULL, etc., establish the connection via OR circuit.

For the target board using NMI, set up the circuitry that allows NMI signal the target board to be cut off with jumper pin, etc. when debugging.

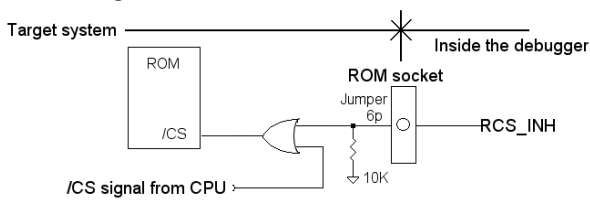
● Other signals

-Status signals (ST1 - ST5)

Pin No.	Signal	Connection
8	ST1	Connect CPU /RD2 signal. (Standard connection)
4	ST2	Connect CPU /WR signal. (Standard connection)
3	ST3	NC (Standard connection)
2	ST4	Status signal of your choice
1	ST5	/EMLIR (Recommended)

Connect signals to be traced as status signals when using tracing/event feature. Standard connection is the one that we recommend among the trace connection patterns available. By ordinary, trace data is captured at /RD2 signal connected to ST1 pin as trace clock. /RD2 signal connection is essential when tracing/event feature is to be used. In Standard connection, it generates trace clock with combination of patterns from Status signals ST1 - ST3 pins, and then captures trace data at the trace clock. The advantage of using Standard connection is that it allows capturing of trace data at timings of signals other than Read (/RD2) signal (timings of Read and Write). In Standard connection, the connection patterns given to the left are recommended. For ST5 pin, it is recommended that you connect /EMLIR signal. It is useful to have the environment that allows implementation of test pin and clipping on the target board.

-CS\_INH signal

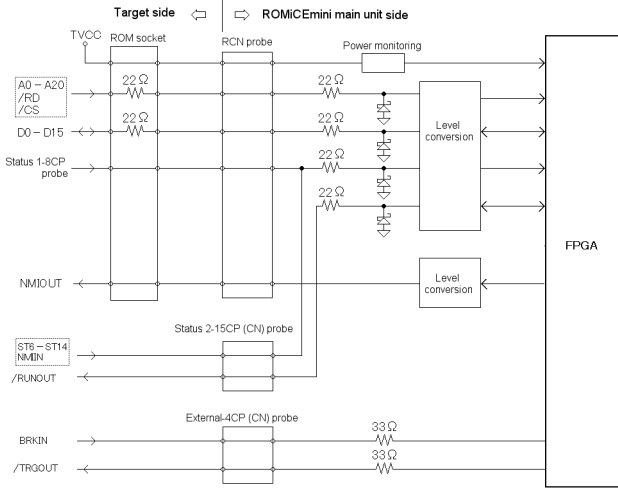


The signal to be output from CS\_INH pin is the output signal for inhibiting access to the ROM on the target board mapped to the same address as emulation ROM area for ROMiCEmini during debugging (while ROMiCEmini is being connected), and always at "H" level. For example, when FLASH ROM directly mounted on the target board and emulation ROM for ROMiCEmini are in the same area, the signal is to be used for inhibiting Flash ROM signal on the target by making OR connections for CS signal and CS\_INH signal of FLASH ROM beforehand so that they do not conflict with each other.

The connection is not necessary if the case is not applicable, for example, where the conflict can be avoided by inserting/removing ROM with ROM socket.

Target interface Specifications (Timing specifications)

● Target interface block diagram



• Input signal

All signals except for BRKIN signal supports 1.8V - 5V. VIH and VIL are as follows.

Target voltage	VIH	VIL
1.8V - 1.95V	VCCx0.7V and higher	VCCx0.3V and lower
2.3V - 2.7V	1.7V and higher	0.7V and lower
2.7V - 5V	2V and higher	0.8V and lower

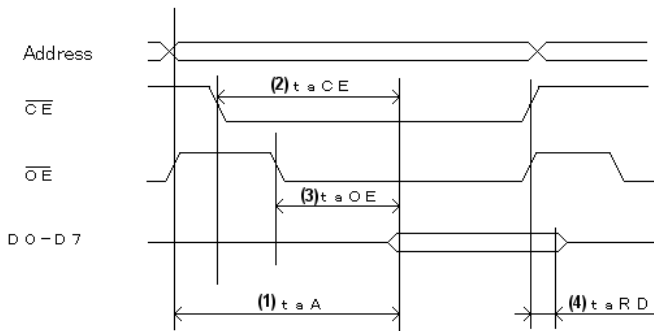
BRKIN signal supports 2.7V - 3.6V. VIH and VIL are as follows.

Target voltage	VIH	VIL
2.7V - 3.6V	2V and higher	0.8V and lower

• Output signal

D0 - D15 and CS\_INH signals are supported between 1.8V-3.3V. They are output at the electric potential adapted for TVCC, the target power. The electric potential over 3.3V will not be output. NMIOUT signal is supported between 1.8V-5V. It is output from the buffer that operates by the target power, at electric potential the same as the target. Be aware that for NMIOUT signal setting, open-collector output is also accepted. /RSTOUT signal is an open-collector output from the transistor. /TRGOUT signal is output at electric potential of 3.3V.

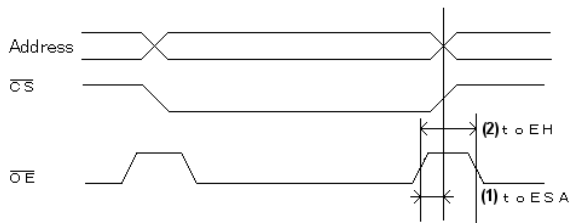
● Emulation ROM access timing



\*: Emulation ROM is an alternate memory incircuited within ROMiCEmini main unit and used as memory to substitute memory on the target board.

Symbol	MIN	MAX	Description
(1) $t_{aA}(\overline{CE}=\overline{OE}=\text{GND})$	-	50ns	Address access time
(2) $t_{aCE}(\overline{OE}=\text{GND})$	-	50ns	/CE access time
(3) $t_{aOE}(\overline{CE}=\text{GND})$	-	35ns	/RD access time
(4) $t_{aRD}$	-	25ns	/RD output disabled time

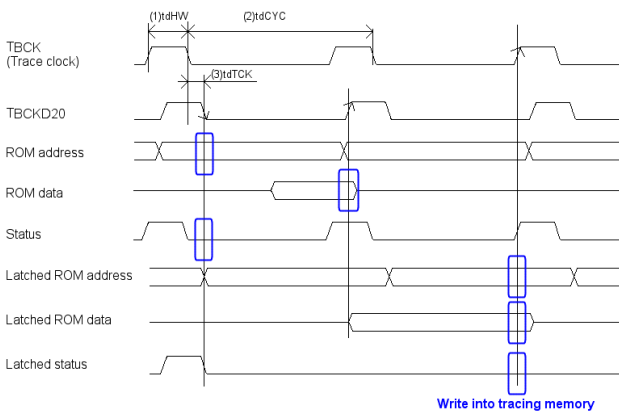
● ROM socket access timing



Specifications	MIN	MAX	Remarks
(1) $t_{oESA}$	0ns	-	-
(2) $t_{oEH}$	10ns	-	It always must be the pulse signal.

\* When ROMiCEmini is to be operated in ROMICE mode, it must satisfy the above timings.

● Trace timing



Specifications	MIN	MAX	Remarks
(1) $t_{dHW}$	10ns	-	-
(2) $t_{dCYC}$	50ns	-	-
(3) $t_{dTCK}$	20ns	-	-

ROMiCEmini latches at the timings of rising and trailing of TBCKD20 approx. 20ns delayed from trace clock (TBCK) and writes, at rising edge of trace clock (TBCK), into tracing memory.

The timings for sampling of each signal are in the following 2 patterns:

- Signal to be sampled at rising edge of TBCKD20
  - Data from ROM
- Signals to be sampled at trailing edge of TBCKD20
  - Addresses from ROM
  - ST1 - 14

\*: The upper limit value of trace clock is 20MHz. However, it may not be supported in some cases depending on the duty ratio of the clock.

Target Interface Specifications (Specifications of connectors for expansion)

●STCN connector

STCN connector is the connector for connecting status signals for tracing/event, and it is to be connected with Status2-15CP probe (Clip type) or Status2-15CN probe (Connector type). Both of the probes are optional.

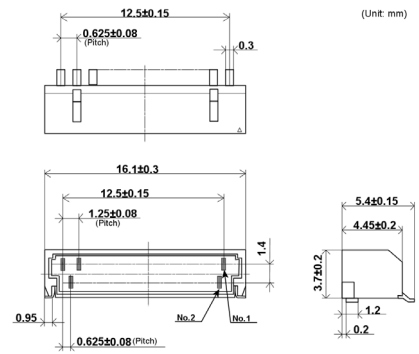
If you intend to connect Status 2-15CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect Status 2-15CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

For ST6 - ST14 pins, signals are to be connected if you are to use tracing/event feature. Connect the signals to be traced at your own discretion.

The connection is not required if you do not intend to use it.

Also, as standard connection pattern, which we recommend, connect the signals in the table below.



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No.	Pin	Input/Output	Input/Output	No.	Pin	Input/Output	Name of signals to be connected
1	ST6	Output	/CS0	2	GND	Output	GND
3	ST7		/CS1	4	GND		
5	ST8		/CS2	6	GND		
7	ST9		/CS3	8	GND		
9	ST10		/CS4	10	GND		
11	ST11		/CS5	12	GND		
13	ST12		NC	14	GND		
15	ST13		NC	16	GND		
17	ST14		NC	18	GND		
19	NMIIN		Output	NMIIN <sup>1)</sup>	20		
21	/RUNOUT	Input	/RUNOUT <sup>2)</sup>				

<sup>1)</sup>Input and output are stated from the target board's point of view.

\*1: For NMIIN pin, connect the NMI signal generated on the target board. Go-Break is implemented at NMIOUT output from ROMiCEmini, but target NMI signal can be used by connecting NMI signal of the target board to NMIIN pin. Set up the circuitry that allows NMI signal on the target board and NMIOUT signal output from ROMiCEmini to be cut off with jumper pin, etc. when debugging.  
The connection is not necessary if you do not use it.

\*2: /RUNOUT signal is a negative logic signal output from ROMiCEmini. It is output at "L" during execution of the user program.  
If output at "H", it means that the user program is in break. The connection is not necessary if you do not use it.

●EXTCN connector

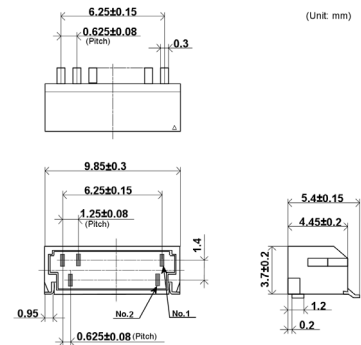
EXTCN connector is the connector for connecting /TRGOUT, BRKIN signals, and it is to be connected with External-4CP probe (Clip type) or External-4CN probe (Connector type). Both of the probes are optional.

If you intend to connect External-4CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect External-4CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

/TRGOUT pin outputs /TRGOUT signal of 1 pulse (negative logic) from ROMiCEmini if matched with the specified condition during the user program execution. The output voltage is at 3.3V. The connection is not required if you do not intend to use it.

BRKIN pin inputs the signal for external force break from outside. It is to be used when you wish to break the user program by external signal of your choice. The setting can be switched between the edges, rising or trailing. The connection is not required if you do not intend to use it.



Japan Aviation Electronics Industry, Ltd. : FI-W11P-HF

No.	Pin	Input/Output	Name of signals to be connected	No.	Pin	Input/Output	Name of signals to be connected
1	/TRGOUT	Input	/TRGOUT	2	GND	Output	GND
3	NC	-	-	4	GND		
5	NC	-	-	6	GND		
7	NC	-	-	8	GND		
9	BRKIN	Output	BRKIN	10	GND		
11	+5.0V	Input	Power*				

\*\*+5.0V power is supplied from ROMiCEmini main unit. By ordinary, leave it unconnected.

\*Input and output are stated from the target board's point of view.