

ROMiCEmini Technical Information

Applicable Product	Supported CPU
ROMiCEmini(16M161)	(Renesas-made) H8/300H series, H8S series

As patterns of the target interface connection for ROMiCEmini, the style using RCN connector connection which allows simplified connection, and the existing style using ROM socket connection are available; establish connection by employing either of the patterns.

Target Interface Specifications (RCN connector connection style)

Dedicated RCN connector signal table

Input and output are stated from the target board's point of view.

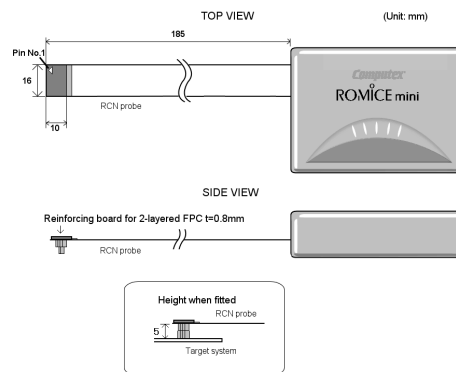
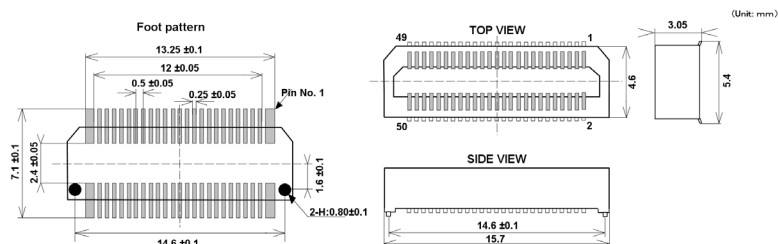
No.	Pin name	Input/Output	Name of signals to be connected	No.	Pin name	Input/Output	Name of signals to be connected
1	TVCC	Output	Power (+1.8V - +5.0V)	2	A0	Output	A0
3	A1	Output	A1	4	A2	Output	A2
5	A3	Output	A3	6	A4	Output	A4
7	A5	Output	A5	8	A6	Output	A6
9	A7	Output	A7	10	A8	Output	A8
11	A9	Output	A9	12	A10	Output	A10
13	A11	Output	A11	14	A12	Output	A12
15	A13	Output	A13	16	A14	Output	A14
17	A15	Output	A15	18	A16	Output	A16
19	A17	Output	A17	20	A18	Output	A18
21	A19	Output	A19	22	A20	Output	A20
23	D0	Input/Output	D0	24	D1	Input/Output	D1
25	D2	Input/Output	D2	26	D3	Input/Output	D3
27	D4	Input/Output	D4	28	D5	Input/Output	D5
29	D6	Input/Output	D6	30	D7	Input/Output	D7
31	D8	Input/Output	D8	32	D9	Input/Output	D9
33	D10	Input/Output	D10	34	D11	Input/Output	D11
35	D12	Input/Output	D12	36	D13	Input/Output	D13
37	D14	Input/Output	D14	38	D15	Input/Output	D15
39	/CE1 ^{*1}	Output	ROMiCEmini CS signal	40	/OE	Output	/RD
41	/BYTE_CE2	Output	NC	42	ST1	Output	NC
43	/RSTOUT ^{*2}	Input	/RSTOUT signal	44	CS_INH ^{*3}	Input	CS_INH signal
45	NMIOUT ^{*2}	Input	NMIOUT signal	46	ST2 ^{*4}	Output	/WRH
47	ST3 ^{*4}	Output	/WRL	48	ST4	Output	NC
49	ST5 ^{*5}	Output	A21	50	GND	Output	GND

The connection style which uses the dedicated RCN connector instead of ROM socket in connection. Being the size of connector small, it has advantages in that the space it occupies is minimal, the connection is simple, ...etc. At the stage of designing the target board, prepare RCN connector and connect the CPU signals or equivalent under Name of signals to be connected.

- *1: For /CE1 pin, connect CS signals of the area for mapping emulation ROM. By ordinary, /CS0, the signal of the area with vector address, is to be connected.
- *2: The signals to be connected to /RSTOUT and NMIOUT pins are essential. See below.
- *3: CS_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. See below for details.
- *4: For ST2 - ST3 pins, connect the signals if you are to use tracing/event feature. See below for details.
- *5: For ST5 pin, connect the signal if you are to use tracing/event feature. The signal to be connected can be determined at your own discretion, yet it is recommended that you connect A21 signal of CPU.

Target Connector Specifications

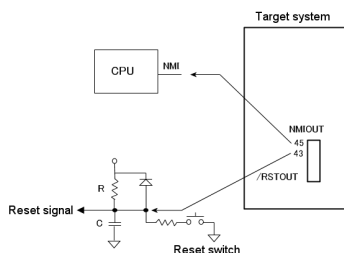
TOKYO ELETECH CORPORATION: SICA2P50S05



When preparing the dedicated RCN connector on the target board, consult the dimensional drawing given above. The connector to be implemented on the target board does not accompany the product. For information on the connector, please contact Tokyo Eletech Corporation.

Essential signals

•/RSTOUT, NMIOUT signals



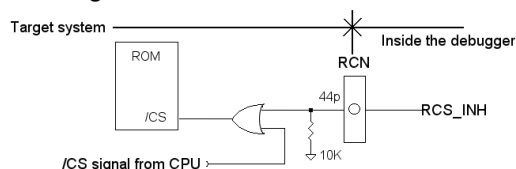
To launch CSIDE and implement Go-Break, /RSTOUT and NMIOUT, the output signals from ROMiCEmini, need to be connected. As shown to the left, connect /RSTOUT and NMIOUT pins of RCN connector to the circuit on the target board. /RSTOUT and NMIOUT signals are open-collector output from ROMiCEmini. Where possible, establish wired OR connection to the RESET circuit on the target board as shown in the drawing. If the RESET circuit on the target board is of COMS-PUSHPULL, etc., establish the connection via OR circuit. For the target board using NMI, set up the circuitry that allows NMI signal on the target board to be cut off with jumper pin, etc. when debugging.

Other signals

•Status signals (ST1 - ST5)

RCN No.	Pin	Connection
42	ST1	The signal of /OE pin is to be connected by internal operation.
46	ST2	Connect CPU /WRH signal. (Standard connection)
47	ST3	Connect CPU /WRL signal. (Standard connection)
48	ST4	NC (In the case of 16-bit bus, A0 is to be connected by internal operation.)
49	ST5	A21 (Recommended)

•CS_INH signal



Connect signals to be traced as status signals when using tracing/event feature. Standard connection is the one that we recommend among the trace connection patterns available. By ordinary, trace data is captured at the signal of /OE pin connected to RCN connector as trace clock. In Standard connection, it generates trace clock with combination of patterns from Status signals ST1 - ST3 pins, and then captures trace data at the trace clock. The advantage of using Standard connection is that it allows capturing of trace data at timings of signals other than Read (timings of Read and Write). In Standard connection, the connection patterns given to the left are recommended. For ST1 pin, you do not need to connect a signal because the signal of /OE pin is to be connected by ROMiCEmini internal operation.

The signal to be output from CS_INH pin is the output signal for inhibiting access to the ROM on the target board mapped to the same address as emulation ROM area for ROMiCEmini during debugging (while ROMiCEmini is being connected), and always at "H" level. For example, when FLASH ROM directly mounted on the target board and emulation ROM for ROMiCEmini are in the same area, the signal is to be used for inhibiting Flash ROM signal on the target by making OR connections for CS signal and CS_INH signal of FLASH ROM beforehand so that they do not conflict with each other. The connection is not necessary if the case is not applicable, for example, where the conflict can be avoided by inserting/removing ROM with ROM socket.

Target Interface Specifications (ROM socket connection style)

● ROM socket signal table

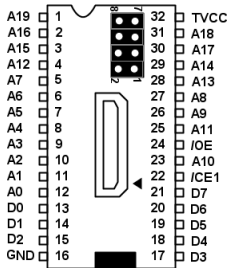
Input and output are stated from the target board's point of view.

- *1: The signals to be connected to /RSTOUT and NMIOUT pins are essential. See below.
- *2: CS_INH pin is to be used for inhibiting access to the memory on the target in the same CS area as ROMiCEmini. See below for details.

*3: For ST1 - ST5 pins, connect the signals if you are to use tracing/event feature. See below for details.

*4: Address signals to be connected to ROM socket varies depending on the bus width. In the case of 8-bit bus, start from A0 of CPU in connecting the signals. In the case of 16-bit bus, start from A1 of CPU in connecting the signals.

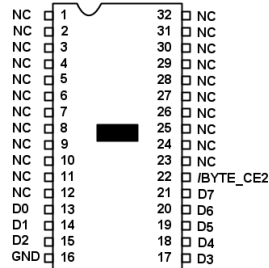
32-pin ROM MAIN socket



Terminal		
Pin	Input/Output	Description
A ₀ - A ₁₉	Output	Address signals
D ₀ - D ₇	Input/Output	Data signals
/CE1	Output	/CS signal
/OE	Output	/RD signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

Jumper			
No.	Pin	Input/Output	Description
1	ST5 ³	Output	Status signals
2	ST4 ³		
3	ST3 ³		
4	ST2 ³		
5	NMIOUT ¹	Input	NMIOUT signal
6	CS_INH ²	Input	CS_INH signal
7	/RSTOUT ¹	Input	/RSTOUT signal
8	ST1 ³	Output	Status signal

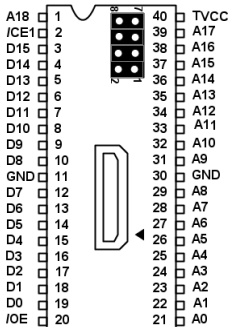
32-pin ROM SUB socket



Terminal		
Pin	Input/Output	Description
NC*	-	-
D ₀ - D ₇	Input/Output	Data signals
/BYTE_CE2	Output	/CS signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

*Even if signals such as address are connected to NC, it does not matter.

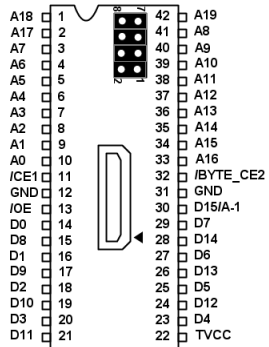
40-pin ROM socket (JEDEC type)



Terminal		
Pin	Input/Output	Description
A ₀ - A ₁₈	Output	Address signals
D ₀ - D ₁₅	Input/Output	Data signals
/CE1	Output	/CS signal
/OE	Output	/RD signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

Jumper			
No.	Pin	Input/Output	Description
1	ST5 ³	Output	Status signals
2	ST4 ³		
3	ST3 ³		
4	ST2 ³		
5	NMIOUT ¹	Input	NMIOUT signal
6	CS_INH ²	Input	CS_INH signal
7	/RSTOUT ¹	Input	/RSTOUT signal
8	ST1 ³	Output	Status signal

42-pin ROM socket (MASK type)

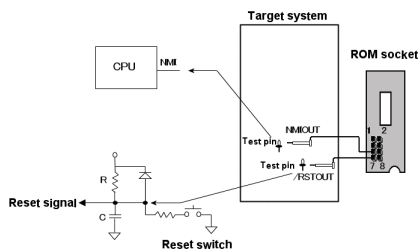


Terminal		
Pin	Input/Output	Description
A ₀ - A ₁₉	Output	Address signals
D ₀ - D ₁₅	Input/Output	Data signals
/CE1	Output	/CS signal
/BYTE_CE2	Output	Switching between 16bit/8bit
/OE	Output	/RD signal
TVCC	Output	Power (+1.8 - +5.0V)
GND	Output	GND

Jumper			
No.	Pin	Input/Output	Description
1	ST5 ³	Output	Status signals
2	ST4 ³		
3	ST3 ³		
4	ST2 ³		
5	NMIOUT ¹	Input	NMIOUT signal
6	CS_INH ²	Input	CS_INH signal
7	/RSTOUT ¹	Input	/RSTOUT signal
8	ST1 ³	Output	Status signal

● Essential signals

• /RSTOUT, NMIOUT signals



To launch CSIDE and implement Go-Break, /RSTOUT and NMIOUT, the output signals from ROMiCEmini, need to be connected.

Connect Status 1-8CP probe (200mm) to the jumper pins of ROM socket, and connect the 2 probes to each pin on the target board as shown to the left. Status1-8CP probe has clips at the end. It will be useful if the target board is implemented with the test pin in advance.

/RSTOUT and NMIOUT signals are open-collector output from ROMiCEmini.

Where possible, establish wired OR connection to the RESET circuit on the target board as shown in the drawing.

If the RESET circuit on the target board is of COMS-PUSH/PULL, etc., establish the connection via OR circuit.

For the target board using NMI, set up the circuitry that allows NMI signal on the target board to be cut off with jumper pin, etc. when debugging.

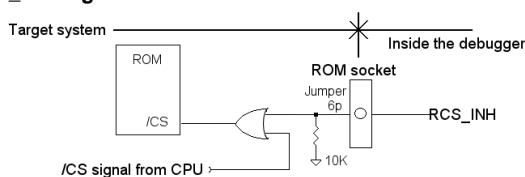
● Other signals

• Status signals (ST1 - ST5)

Pin No.	Signal	Connection
8	ST1	Connect CPU /RD signal. (Standard connection)
4	ST2	Connect CPU /WRH signal. (Standard connection)
3	ST3	Connect CPU /WRL signal. (Standard connection)
2	ST4	Status signal of your choice
1	ST5	Status signal of your choice

Connect signals to be traced as status signals when using tracing/event feature. Standard connection is the one that we recommend among the trace connection patterns available. By ordinary, trace data is captured at the signal of /OE pin connected to ROM socket as trace clock. In standard connection, it generates trace clock with combination of patterns from Status signals ST1 - ST3 pins, and then captures trace data at the trace clock. The advantage of using Standard connection is that it allows capturing of trace data at timings of signals other than Read (timings of Read and Write). In standard connection, the connection patterns given to the left are recommended. It is useful to have the environment that allows implementation of test pin and clipping on the target board.

• CS_INH signal

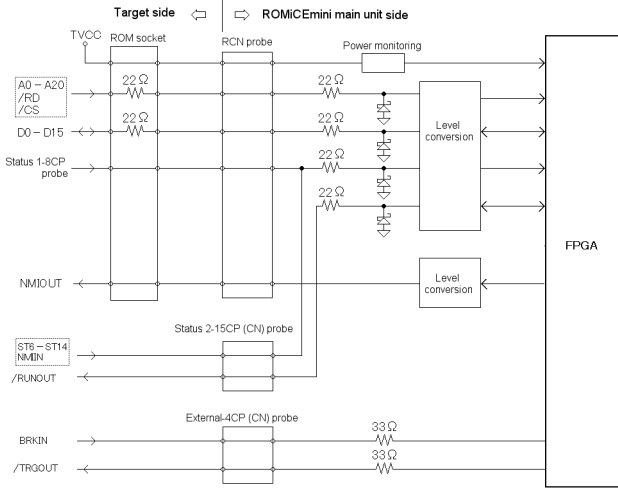


The signal to be output from CS_INH pin is the output signal for inhibiting access to the ROM on the target board mapped to the same address as emulation ROM area for ROMiCEmini during debugging (while ROMiCEmini is being connected), and always at "H" level. For example, when FLASH ROM directly mounted on the target board and emulation ROM for ROMiCEmini are in the same area, the signal is to be used for inhibiting Flash ROM signal on the target by making OR connections for CS signal and CS_INH signal of FLASH ROM beforehand so that they do not conflict with each other.

The connection is not necessary if the case is not applicable, for example, where the conflict can be avoided by inserting/removing ROM with ROM socket.

Target Interface Specifications (Timing specifications)

● Target interface block diagram



• Input signal

All signals except for BRKIN signal supports 1.8V - 5V. VIH and VIL are as follows.

Target voltage	VIH	VIL
1.8V - 1.95V	VCCx0.7V and higher	VCCx0.3V and lower
2.3V - 2.7V	1.7V and higher	0.7V and lower
2.7V - 5V	2V and higher	0.8V and lower

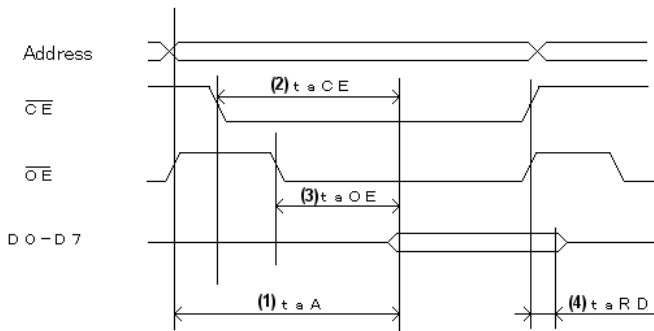
BRKIN signal supports 2.7V - 3.6V. VIH and VIL are as follows.

Target voltage	VIH	VIL
2.7V - 3.6V	2V and higher	0.8V and lower

• Output signal

D0 - D15 and CS_INH signals are supported between 1.8V-3.3V. They are output at the electric potential adapted for TVCC, the target power. The electric potential over 3.3V will not be output. NMIOUT signal is supported between 1.8V-5V. It is output from the buffer that operates by the target power, at electric potential the same as the target. Be aware that for NMIOUT signal setting, open-collector output is also accepted. /RSTOUT signal is an open-collector output from the transistor. /TRGOUT signal is output at electric potential of 3.3V.

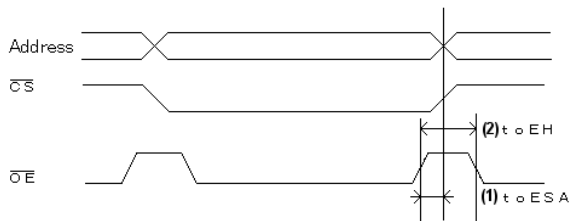
● Emulation ROM access timing



*: Emulation ROM is an alternate memory incircuited within ROMiCEmini main unit and used as memory to substitute memory on the target board.

Symbol	MIN	MAX	Description
(1) $t_{aA}(\overline{CE}=\overline{OE}=\text{GND})$	-	50ns	Address access time
(2) $t_{aCE}(\overline{OE}=\text{GND})$	-	50ns	/CE access time
(3) $t_{aOE}(\overline{CE}=\text{GND})$	-	35ns	/RD access time
(4) t_{aRD}	-	25ns	/RD output disabled time

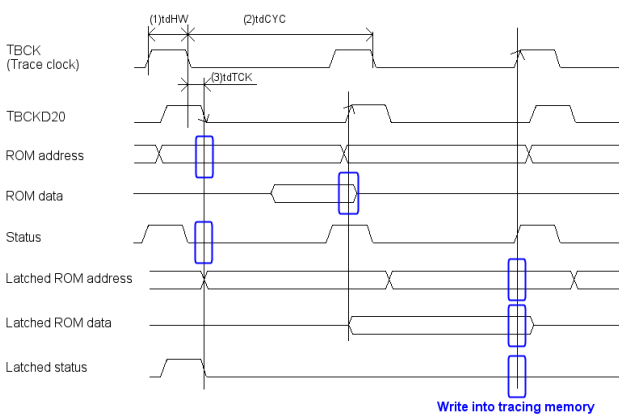
● ROM socket access timing



Specifications	MIN	MAX	Remarks
(1) t_{oESA}	0ns	-	-
(2) t_{oEH}	10ns	-	It always must be the pulse signal.

* When ROMiCEmini is to be operated in ROMICE mode, it must satisfy the above timings.

● Trace timing



Specifications	MIN	MAX	Remarks
(1) t_{dHW}	10ns	-	-
(2) t_{dCYC}	50ns	-	-
(3) t_{dTCK}	20ns	-	-

ROMiCEmini latches at the timings of rising and trailing of TBCKD20 approx. 20ns delayed from trace clock (TBCK) and writes, at rising edge of trace clock (TBCK), into tracing memory.

The timings for sampling of each signal are in the following 2 patterns:

- Signal to be sampled at rising edge of TBCKD20
 - Data from ROM
- Signals to be sampled at trailing edge of TBCKD20
 - Addresses from ROM
 - ST1 - 14

*: The upper limit value of trace clock is 20MHz. However, it may not be supported in some cases depending on the duty ratio of the clock.

Target Interface Specifications (Specifications of connectors for expansion)

● STCN connector

STCN connector is the connector for connecting status signals for tracing/event, and it is to be connected with Status2-15CP probe (Clip type) or Status2-15CN probe (Connector type). Both of the probes are optional.

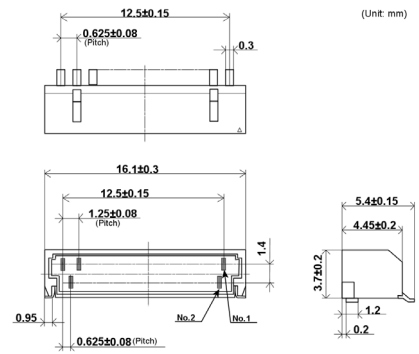
If you intend to connect Status 2-15CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect Status 2-15CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

For ST6 - ST14 pins, signals are to be connected if you are to use tracing/event feature. Connect the signals to be traced at your own discretion.

The connection is not required if you do not intend to use it.

Also, as standard connection pattern, which we recommend, connect the signals in the table below.



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No.	Pin	Input/Output	Name of signals to be connected	No.	Pin	Input/Output	Name of signals to be connected
1	ST6	Output	/CS0	2	GND	Output	GND
3	ST7		/CS1	4	GND		
5	ST8		/CS2	6	GND		
7	ST9		/CS3	8	GND		
9	ST10		/CS4	10	GND		
11	ST11		/CS5	12	GND		
13	ST12		NC	14	GND		
15	ST13		NC	16	GND		
17	ST14		NC	18	GND		
19	NMIIN		Output	NMIIN ¹	20		
21	/RUNOUT	Input	/RUNOUT ²				

¹ Input and output are stated from the target board's point of view.

*1: For NMIIN pin, connect the NMI signal generated on the target board. Go-Break is implemented at NMIOUT output from ROMiCEmini, but target NMI signal can be used by connecting NMI signal of the target board to NMIIN pin. Set up the circuitry that allows NMI signal on the target board and NMIOUT signal output from ROMiCEmini to be cut off with jumper pin, etc. when debugging. The connection is not necessary if you do not use it.

*2: /RUNOUT signal is a negative logic signal output from ROMiCEmini. It is output at "L" during execution of the user program. If output at "H", it means that the user program is in break. The connection is not necessary if you do not use it.

● EXTCN connector

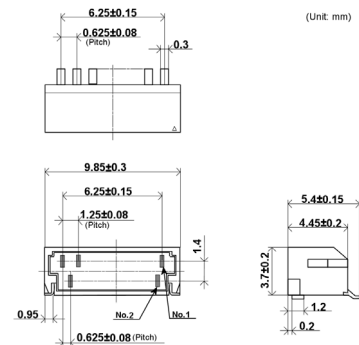
EXTCN connector is the connector for connecting /TRGOUT, BRKIN signals, and it is to be connected with External-4CP probe (Clip type) or External-4CN probe (Connector type). Both of the probes are optional.

If you intend to connect External-4CP probe (Clip type), preparing test pins on the target board will be useful.

If you intend to connect External-4CN probe (Connector type), prepare the prescribed connector on the target board. It will allow simplified connection.

/TRGOUT pin outputs /TRGOUT signal of 1 pulse (negative logic) from ROMiCEmini if matched with the specified condition during the user program execution. The output voltage is at 3.3V. The connection is not required if you do not intend to use it.

BRKIN pin inputs the signal for external force break from outside. It is to be used when you wish to break the user program by external signal of your choice. The setting can be switched between the edges, rising or trailing. The connection is not required if you do not intend to use it.



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No.	Pin	Input/Output	Name of signals to be connected	No.	Pin	Input/Output	Name of signals to be connected
1	/TRGOUT	Input	/TRGOUT	2	GND	Output	GND
3	NC	-	-	4	GND		
5	NC	-	-	6	GND		
7	NC	-	-	8	GND		
9	BRKIN	Output	BRKIN	10	GND		
11	+5.0V	Input	Power				

* +5.0V power is supplied from ROMiCEmini main unit. By ordinary, leave it unconnected.

* Input and output are stated from the target board's point of view.