

Applicable Product  
F-SightXstick MicroBlaze

Target Interface Specifications

Signal table of TARGET connector on F-SightXstick side

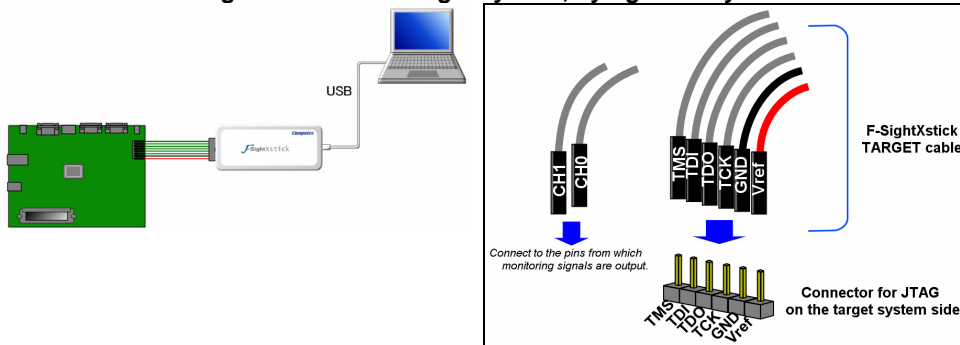
No.	Signal	Input/Output <sup>1</sup>	No.	Signal	Input/Output <sup>1</sup>
1	N.C.		2	CH1	Output
3	N.C.		4	CH0	Output
5	N.C.		6	N.C.	
7	N.C.		8	TDO	Output
9	N.C.		10	N.C.	
11	N.C.		12	TCK	Input
13	N.C.		14	TMS	Input
15	N.C.		16	TDI	Input
17	GND		18	N.C.	
19	N.C.		20	Vref <sup>2</sup>	Output

\*: For pins where stated as N.C., leave signals unconnected.

\*1: Input/output is based on the target.

\*2: Apply the reference voltage of JTAG signal (TMS/TDI/TDO/TCK) interface. For example, in the case of Virtex-II Pro, connect VCCAUX voltage (2.5V). It is to serve for potential detection, and pull-up signal of around 1KΩ will do.

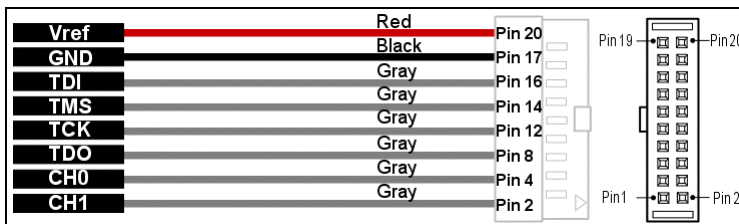
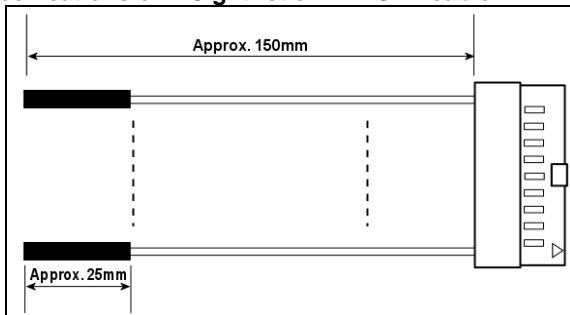
For connection of F-SightXstick to the target system, flying-wire style cable is to be used.



Each of F-SightXstick TARGET cable ends has been written with the signal name. Connect each of them to the pin of JTAG connector on the target system from which the signals are output.

CH0 and CH1 are analyzer signals for wave pattern monitoring. The connections are not required if you do not intend to use analyzer feature.

Specifications of F-SightXstick TARGET cable

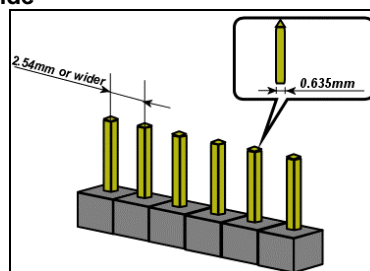


Pin No.	Signal	The colour of cables
20	Vref	Red
17	GND	Black
16	TDI	Gray
14	TMS	Gray
12	TCK	Gray
8	TDO	Gray
4	CH0	Gray
2	CH1	Gray

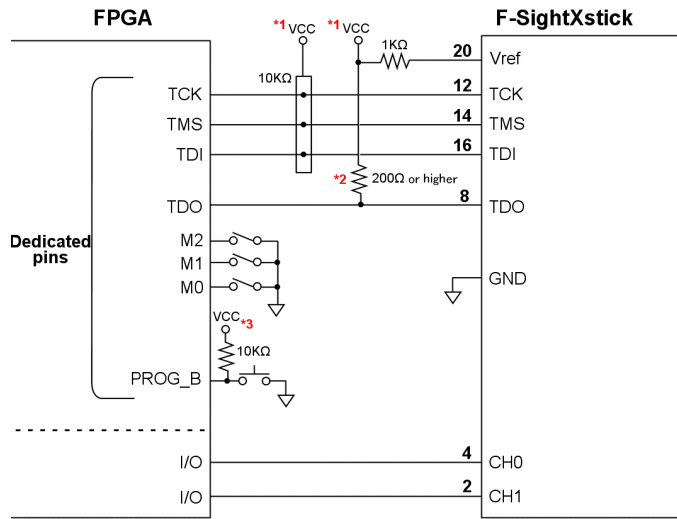
Pins other than those mentioned above will be left N.C.

Specifications of the header on the target system side

Pitch: 2.54mm (0.10 inch) or wider pitch  
Pins: 0.635mm (0.025 inch) or equivalent pin



Target Connection Reference Diagram



**\*1:** The voltage value for FPGA configuration varies from device to device. Refer to the data book for the device you use. F-SightXstick supports 2.5V and 3.3V.

**\*2:** In the case of Virtex II Pro, it requires pull-up resistor for TDO signal. Resistors of 200 ohm or higher are recommended by Xilinx.

**\*3:** For FPGA devices not internally implemented with pull-up register for PROG\_B signal, PROG\_B signal line needs to be equipped with external pull-up resistor. As for power and voltage of external pull-up register, refer to the data book for the device you use.

- Set FPGA configuration mode to M2:M1:M0=1:0:1 when you use F-SightXstick.
- F-SightXstick does not support writing via JTAG interface to a write-access-enabled PROM for configuration. If the configuration PROM is connected to JTAG signal line, arrange another connector supporting the writing tool.
- FPGA may not be reconfigured correctly in some cases depending on the JTAG daisy chained state of your devices. Therefore, we advise you to prepare a switch for PROG\_B signal line.