This document consists of the following contents.

 Technical Information on JTAG / SWD / SWV / ETM ARM-related Target Interface (12th Edition)

Refer this document before using PALMiCE4-ARM.

PALMiCE4 Hardware Manual (11th Edition)
 Target interface Specifications on PALMiCE4 side.

Technical Information ARM-related JTAG / SWD / SWV / ETM Target Interfaces

12th Edition (Jan. 22, 2025)

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Document change history

First Edition	Sep. 11, 2009	Initial edition
Second Edition	Nov. 13, 2009	Added the descriptions on CPU core "ARM" and "PALMiCE3 ARM (JTAG200)" to Technical
		Information reference chart and Product purchase chart.
		Corrected the Product purchase chart.
		Technical Information ④ and ⑥ correspond to PALMiCE3 CM3 (ETM200) only.
		However, PALMiCE3 CM3(ETM200) is a product to be released in the future.
		 Added the note on SRST signal in respective signal tables.
		"SRST signal is an open-collector output."
Third Edition	Mar. 04, 2011	PALMiCE3 CM3(ETM200) has already been released (Dec. 2009).
		Deleted the following description:
		" To be released in the future."
		Supported connectors
		Added graphic images of the connectors.
		Product purchase chart Added graphic imposes of the entired products
		Added graphic images of the optional products.
		- Added the note on TDST signal in respective signal tables.
		Changed the hole of TRST signal intespective signal tables.
		chart
		For supported CPUs, refer to Product Summary of respective products up on our website
		Deleted the description of the case where FTM is not used and half-pitch (1.27mm) connector is
		used.
		When you use them, please contact us.
Fourth Edition	Sep. 18, 2015	Added an item to Applicable products:
		PALMICE2H ARM (ETM383)
		• Following addition of an item to Applicable products mentioned above, added the description on
		PALMiCE2H to Technical Information reference chart and Product purchase chart.
		• Following addition of an item to Applicable products mentioned above, added ⑦⑧⑪ to
		pages on target interface details.
		Placed specifications of the target interface on the debugger side.
		PALMICE3 PALMICE3 JTAG200 model Hardware Manual)
		PALMICE2H Extracted from PALMICE2H ARM User's Manual)
		Supported connectors – 38-pin Mictor connector
		Changed the recommended connectors.
		[Define change] 2-767004-2/767034-1/767001 (Kons-non-compliant products)
		Supported connectors
		Added the note
		Product nurchase chart
		Added "PALMICE3-ARM (JTAG200)" to (7) to (10.
		• Added notes on the TRST signal described in (2) (Using 20-pin 2.54 mm-pitch connector +
		JTAG interface).
		Added ⑥ (Using 20-pin 1.27 mm-pitch connector + JTAG interface).
		• According to the above addition, incremented the heading number (6) and subsequent numbers
		by one.
		• In accordance with J-STICK sales termination, deleted J-STICK descriptions from the applicable
		products and the product purchase chart.
Fifth Edition	Mar. 04, 2016	In accordance with PALMiCE3 CM3(ETM200) sales termination, deleted PALMiCE3
		CM3(ETM200) descriptions from the applicable products and the product purchase chart.
		Product purchase chart
		Added "PALMiCE3 CM3(JTAG200)" to ①, ②, ③, ⑥, ⑦, ⑧, ⑨, ⑩ and ⑪.
		Added an item to Applicable products:
		PALMiCE3 CM3(JTAG200)
		• Added a note that SWO signal is unused in (1) , (3) and (7) .
Sixth Edition	Oct. 30, 2018	Updated Table of contents
		• About ②, ⑥, ⑪
		 Annotation added for TRST, SRST signals
		 TRST signal related changes in the Target connection reference diagram
		Reference note added for RZ/A and RZ/T series /SRST, /TRST signals
		Added ⑧ (Using 10-pin 1.27 mm-pitch connector + JTAG interface).
		• According to the above addition, incremented the heading number (8) and subsequent numbers
		by one.

Seventh Edition	lun 25 2021	Added new products
Coventin Edition	0011. 20,2021	DAL MCC4 ARM (Model I)
		PALMICE+-ARM64 (Model)
		PALMICETACM (Model)
		PALMICE4-OBM (Model-5)
		PALMICE4-ARMANNI (MODELT)
		PALMICE4-ARMO4-IMI (Model-1)
		PALMICE4-CWI-WI (MODEL-1)
		Deleted discontinued product.
		PALMICE2H-ARM (ETM383)
		 "Product combination" changed to "Product combination – PALMiCE3". "Product combination – PALMiCE4".added
		Deleted the old interface specification of 38-pin Mictor connector.
		JTAG interface + ETM – normal mode
		JTAG interface + ETM – Demulti mode
		JTAG interface + ETM – multiplex mode
		Added interface specifications of the 38-pin Mictor connector.
		Added SWD interface + Trace
		Discontinued products have been deleted
		PALMICE3-ARM related products
		Updated the target reference circuit diagram
		No.(1)~(10)
		• Added note about V/Tref
		No Q~m
		Added note about Trace interface
	1	
Eighth Ealtion	Jan. 27, 2022	Updated the signal table and added a note about Reserve.
		No.(1)(2)
		Updated the target reference schematic.
		No.①②
Ninth Edition	May. 15, 2023	 Added a link about "chw585_p4_etmtrace_if.pdf (Japanese document)" in the text.
Tenth Edition	Feb. 05, 2024	• The pins 11 and 13 in the target reference circuit diagram have been changed to N.C.
		No.34
11th Edition	Jun. 28. 2024	Updated Technical Information reference chart and Product combination contents
	*	Added No ① and No ⑦
		• Added description of pins 11 and 13
		No @~@
		No. W W
10th Edition	lan 00 0005	Audeu About Optional Conversion Probes .
12th Ealtion	Jan. 22, 2025	Updated the signal table
		No.(5)(6)(8)

Supported connectors



* Please look at the pin configuration diagram and make sure that the connector is in the right direction before connecting.

Moreover, please check the pin number in the corresponding signal table and make sure the signal and the pin numbers match.

Applicable products

This manual is applicable for the following products.

- PALMiCE4-ARM (Model-J)
- PALMiCE4-ARM64 (Model-J)
- PALMiCE4-CM (Model-J)
- PALMiCE4-ARM-MI (Model-T)
- PALMiCE4-ARM64-MI (Model-T)
- PALMiCE4-CM-MI (Model-T)

Technical Information reference chart

Depending on the target interface you use, Technical Information you should refer to will be different. Based on the chart below, consult the applicable Technical Information.



*: Only those combinations available for selection are given. For other combinations, please contact us.

Product combination

The optional products that need to be purchased will depend on the target interface and the connection. Based on the Technical Information No. (See "Technical Information reference chart" on the previous page), choose the required product.



Various optional conversion probes are available for connection in addition to the target interface described above.

For connection to 2mm pitch 14-pin connector on AMD Xilinx boards	PRB-XIL-MIL20-2M14 (CAP3M)
For connection to 14-pin MIL connector on Texas Instruments boards	ADP-ARM-TI (CAP0E)
Discrete connector wire	PRB-MIL20-FLY6SWD (CP02J)
When connecting to the debug I/F connector of a Texas Instruments board (20-pin MICRO SOCKET connector)	ADP-ARM-MIL20-MS20 (CAP2R)
In case of PALMiCE4 (Model-J), the optional isolation adapter can be used in all combinations (Note that RTCK, DBGRQ, and DBGACK signals are not supported).	ADP-ISO-MIL20-MIL20 (CAP3F)

*2: The code in parentheses after the optional product name is the product code. Please use it when looking at the price list on our website.

20-pin 2.54mm-pitch connector

Target connector specifications



Recommended connector Manufacturer: OMRON Corporation Model: XG4C-2031

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.

Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

(1) SWD interface

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref ^{*5}	Output	2	Reserve*3	
3	NC		4	GND	
5	NC		6	GND	
7	SWDIO	Input/Output	8	GND	
9	SWCLK	Input	10	GND	
11	NC		12	GND	
13	SWO ^{*4}	Output	14	GND	
15	SRST*2		16	GND	
17	NC		18	Reserve*6	
19	NC		20	Reserve*6	

*1: The target system side is taken as reference for Input/output. *2: SRST is an open drain output signal.

Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system.

*3: Not used by our debugger; leave it as NC. *4: If the SWV(Serial Wire Viewer) is not used for debugging or the CPU

does not support the SWV, do not connect anything to the SWO signal. *5 Connect to the I/O power supply of the CPU SWD signal.

*6: "Reserve" signal(s) on the debugger could be connected to GND on the target system.

■ This interface does not use TRST. If the target CPU has a TRST pin, connect a pull up resistor of 10K ohm.

Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.



2 JTAG interface

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref ^{*8}	Output	2	Reserve*5	
3	TRST*6 *7	Input	4	GND	
5	TDI	Input	6	GND	
7	TMS	Input	8	GND	
9	TCK	Input	10	GND	
11	RTCK ^{*2}	Output	12	GND	
13	TDO	Output	14	GND	
15	SRST*3 *7	Input	16	GND	
17	DBGRQ*4	Input	18	Reserve ^{*9}	
19	DBGACK*4	Output	20	Reserve*9	

*1: The target system side is taken as reference for Input/output. *2: Leave unconnected if this signal is not present on the CPU or if RTCK

 signal is not used.
 *3: SRST is an open drain output signal. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system. *4: Leave unconnected if this signal is not present on the CPU.

- *5: Not used by our debugger; leave it as NC.
 *6: In some CPUs, a pulldown many be necessary. Refer the CPU datasheet and make the necessary pull up/pull down changes if required. *7: Some precautions are needed for few CPUs made by Renesas
- Electronics. Refer [Reference: RZ/A and RZ/T series /SRST, /TRST reference diagram] for more information.
- *8 Connect to the I/O power supply of the CPU JTAG signal.
- "Reserve" signal(s) on the debugger could be connected to GND on the *9· target system.



Target connection reference diagram

Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.

20-pin 1.27mm-pitch connector

Target connector specifications



Recommended connector Manufacturer: Samtec, Inc. Model: FTSH-110-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.

Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

(Top view on the target board)

3 SWD interface

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref ^{*5}	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO ^{*4}	Output
7	Key*3		8	NC	
9	GND		10	SRST*2	Input
11	GND*6		12	NC	
13	GND*6		14	NC	
15	GND		16	NC	
17	GND		18	NC	
19	GND		20	NC	
*1 · Th	e target evet	om sido is tal	on as re	forence for Ir	put/output

 *1: The target system side is taken as reference for Input/output.
 *2: SRST is an open drain output signal. Establish wired-OR connection to "power-on-reset" or "system

reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system. *3: "Key" is intended for protection against wrong insertion.

- 44: If the SWV(Serial Wire Viewer) is not used for debugging or the CPU does not support the SWV, do not connect anything to the SWO signal.
- *5: Connect to the I/O power supply of the CPU SWD signal.

*6: While leaving it unconnected on the target side, attach ADP-20HP-20HP-1113NC to the tip of SWJ-PRB-MIL20-20HP.

- This interface does not use TRST. If the target CPU has a TRST pin, connect a pull up resistor of 10K ohm.
- Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.



(4) SWD interface + Trace

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref ^{*6}	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO*2	Output
7	Key*5		8	NC	Input
9	GND		10	SRST*3	Input
11	GND*7		12	TraceClk	Output
13	GND*7		14	TraceD0/SWO*4	Output
15	GND		16	TraceD1	Output
17	GND		18	TraceD2	Output
19	GND		20	TraceD3	Output

*1: The target system side is taken as reference for Input/output. *2: Connect the signal dedicated to SWO. If pin 14 is used as SWO signal (refer ***4**), this can be left unconnected. ***3**: SRST is an open drain output signal.

Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V

and matches the circuit of the target system. *4: In some CPUs, SWO and TraceD0 are multiplexed. In the case of such pin, connect SWO signal not to Pin No. 6 but to Pin No.14 even when you intend to use Pin No. 14 as SWO, not as TraceD0.

*5: "Key" is intended for protection against wrong insertion.

*6: Connect to the I/O power supply of the CPU SWD signal.

*7: While leaving it unconnected on the target side, attach ADP-20HP-20HP-1113NC to the tip of SWJ-PRB-MIL20-20HP.

- This interface does not use TRST. If the target CPU has a TRST pin, connect a pull up resistor of 10K ohm.
 Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.
- When using Trace interface, refer chw585 p4 etmtrace if.pdf.



(5) JTAG interface + Trace

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref ^{*4}	Output	2	TMS	Input
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key ^{*3}		8	TDI	Input
9	GND		10	SRST*2	Input
11	GND ^{*5}		12	TraceClk	Output
13	GND ^{*5}		14	TraceD0	Output
15	GND		16	TraceD1	Output
17	GND		18	TraceD2	Output
19	GND		20	TraceD3	Output

*1: The target system side is taken as reference for Input/output.
*2: SRST is an open drain output signal. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system.

*3: "Key" is intended for protection against wrong insertion.

*4: Connect to the I/O power supply of the CPU JTAG signal.

*5: While leaving it unconnected on the target side, attach ADP-20HP-20HP-1113NC to the tip of SWJ-PRB-MIL20-20HP.



This interface does not use TRST. If the target CPU has a TRST pin, connect a pull up resistor of 10K ohm.
 Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.

When using Trace interface, refer <u>chw585_p4_etmtrace_if.pdf</u>.

(6) JTAG interface

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref*7	Output	2	TMS	Input
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key*3		8	TDI	Input
9	GND		10	SRST*2*6	Input
11	GND*8		12	NC	
13	GND*8		14	RTCK*4	Output
15	GND		16	TRST*5*6	Input
17	GND		18	NC	
19	GND		20	NC	

*1: The target system side is taken as reference for Input/output.

 The target system and is target as release for impublication.
 SRST is an open drain output signal.
 Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system.

*3: "Key" is intended for protection against wrong insertion.

- *4: NC If the CPU pin is not present or if RTCK is not used. $^{\star 5}$: In some CPUs, a pulldown many be necessary. Refer the CPU datasheet and make the necessary pull up/pull down changes if reauired.
- Some precautions are needed for few CPUs made by Renesas *6: Electronics. Refer [Reference: RZ/A and RZ/T series /SRST, /TRST reference diagram] for more information.
- *7: Connect to the I/O power supply of the CPU JTAG signal.
- While leaving it unconnected on the target side, attach ADP-20HP-20HP-1113NC to the tip of SWJ-PRB-MIL20-20HP. *8

Target connection reference diagram



Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.

10P connector

10-pin 1.27mm-pitch connector

Target connector specifications



(Top view on the target board)

- Recommended connector
- Manufacturer:Samtec, Inc.

Model: FTSH-105-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.

Target connection reference diagram

Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

SWD interface

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref ^{*5}	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO ^{*4}	Output
7	Key ^{*3}		8	NC	Input
9	GND		10	SRST*2	Input

 *1: The target system side is taken as reference for Input/output.
 *2: SRST is an open drain output signal. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system. *3: "Key" is intended for protection against wrong insertion.

*4: If the SWV(Serial Wire Viewer) is not used for debugging or the CPU does not support the SWV, do not connect anything to the SWO signal.

*5: Connect to the I/O power supply of the CPU SWD signal.

VTref^{*5} 10K gull up SWDIO 4 SWCLK ⁶ swo*4 vçc CPU ¢ 10 ය 10K ς7 pull up Key*3 8 NC GND

VCC-IO

This interface does not use <u>TRST</u>. If the target CPU has a <u>TRST</u> pin, connect a pull up resistor of 10K ohm.

Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.

8 JTAG interface

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	VTref ^{*4}	Output	2	TMS	Input
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key ^{*3}		8	TDI	Input
9	GND		10	SRST*2	Input

*1: The target system side is taken as reference for Input/output.
 *2: SRST is an open drain output signal. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V

and matches the circuit of the target system. *3: "Key" is intended for protection against wrong insertion.

*4: Connect to the I/O power supply of the CPU SWD signal.



Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.

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38-pin Mictor connector

Target connector specifications



(Top view on the target board)

possible to CPU so that wiring pattern length will be minimized. Also in mounting JTAG connector, place it to the position close to Also in mounting JTAG conn ETM connector. In addition, you will need to connect the Grand Bus Leads of ETM connector to Connect to GND -E + + + ->

In mounting ETM connector, place it to the position as close as

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

*Please look at the pin configuration diagram above and make sure that the connector is in the right direction before connecting.

Please check the pin number in the signal table above and make sure the signal and the pin numbers match.

(9) JTAG interface + ETM / PTM

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	TRACECLK	Output
7	DBGRQ*2	Input	8	DBGACK ^{*2}	Output
9	SRST*3*8	Input	10	Reserve	Input
11	TDO	Output	12	VTref ⁴	Output
13	RTCK ^{*5}	Output	14	TVDD*6	Output
15	TCK	Input	16	TRACEDATA[7] *9	Output
17	TMS	Input	18	TRACEDATA[6] *9	Output
19	TDI	Input	20	TRACEDATA[5] *9	Output
21	TRST*7*8	Input	22	TRACEDATA[4] *9	Output
23	Reserve		24	TRACEDATA[3] *9	Output
25	Reserve		26	TRACEDATA[2] *9	Output
27	Reserve		28	TRACEDATA[1] *9	Output
29	Reserve		30	Reserve	Output
31	Reserve		32	Reserve	Output
33	Reserve		34	Reserve	Output
35	Reserve		36	TRACECTL	Output
37	Reserve		38	TRACEDATA[0] *9	Output

*1: The target system side is taken as reference for Input/output.

*2: Leave unconnected if this signal is not present on the CPU. *3: SRST is an open drain output signal. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system.

*4: Connect to the I/O power supply of the CPU JTAG signal.

*5: Leave unconnected if this signal is not present on the CPU or if RTCK signal is not used.

*6: Not used by our debugger; leave it as NC.

*7: In some CPUs, a pulldown many be necessary. Refer the CPU datasheet and make the necessary pull up/pull down changes if required. Some precautions are needed for few CPUs made by Renesas Electronics.

Refer [Reference: RZ/A and RZ/T series /SRST, /TRST reference diagram] for more information.

*9: For the names of signals corresponding to respective pin No., see the table of Signals.

Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.

When using Trace interface, refer chw585 p4 etmtrace if.pdf.



Recommended connector Manufacturer : AMP Model : Mictor connector the GND 2-767004-2 / 767054-1 / 767061

WD interface + Trace

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	TRACECLK	Output
7	Reserve		8	Reserve	
9	SRST*2	Input	10	Reserve	
11	SWO*4	Output	12	VTref ^{*5}	Output
13	Reserve		14	TVDD *3	Output
15	SWCLK	Input	16	TRACEDATA[7]	Output
17	SWDIO	Input/Output	18	TRACEDATA[6]	Output
19	Reserve		20	TRACEDATA[5]	Output
21	Reserve		22	TRACEDATA[4]	Output
23	Reserve		24	TRACEDATA[3]	Output
25	Reserve		26	TRACEDATA[2]	Output
27	Reserve		28	TRACEDATA[1]	Output
29	Reserve		30	Reserve	
31	Reserve		32	Reserve	
33	Reserve		34	Reserve	
35	Reserve		36	Reserve	
37	Reserve		38	TRACEDATA[0]	Output

*1: The target system side is taken as reference for Input/output.
*2: SRST is an open drain output signal. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system.

*3: Not used by our debugger; leave it as NC.

*4: If the SWV(Serial Wire Viewer) is not used for debugging or the CPU does not support the SWV, do not connect anything to the SWO signal.
*5: Connect to the I/O power supply of the CPU SWD signal.

This interface does not use TRST. If the target CPU has a TRST pin, connect a pull up resistor of 10K ohm.

Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.

When using Trace interface, refer <u>chw585 p4 etmtrace if.pdf</u>.



(1) JTAG interface

Signals

Pin	Signal	Input/	Pin	Signal	Input/
INO.		Output	INO.		Output ·
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	Reserve	
7	DBGRQ*2	Input	8	DBGACK*2	Output
9	SRST*3 *8	Input	10	Reserve	
11	TDO	Output	12	VTref ^{*4}	Output
13	RTCK ^{*5}	Output	14	TVDD*6	Output
15	ТСК	Input	16	Reserve	
17	TMS	Input	18	Reserve	
19	TDI	Input	20	Reserve	
21	TRST*7 *8	Input	22	Reserve	
23	Reserve		24	Reserve	
25	Reserve		26	Reserve	
27	Reserve		28	Reserve	
29	Reserve		30	Reserve	
31	Reserve		32	Reserve	
33	Reserve		34	Reserve	
35	Reserve		36	Reserve	
37	Reserve		38	Reserve	

*1: The target system side is taken as reference for Input/output.

- *2: Leave unconnected if this signal is not present on the CPU.
- *3: SRST is an open drain output signal.

Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system. *4: Connect to the I/O power supply of the CPU JTAG signal.

- *5: Leave unconnected if this signal is not present on the CPU or if RTCK signal is not used.

*6: Not used by our debugger; leave it as NC.

- *7: In some CPUs, a pulldown many be necessary. Refer the CPU datasheet and make the necessary pull up/pull down changes if required. *8: Some precautions are needed for few CPUs made by Renesas Electronics.
- Refer [Reference: RZ/A and RZ/T series /SRST, /TRST reference diagram] for more information.
- Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.



(12)SWD interface

Signals

Pin No.	Signal	Input/ Output ^{*1}	Pin No.	Signal	Input/ Output ^{*1}
1	NC		2	NC	
3	NC		4	NC	
5	GND		6	Reserve	
7	Reserve		8	Reserve	
9	SRST*2	Input	10	Reserve	
11	SWO*4	Output	12	VTref ^{*5}	Output
13	Reserve		14	TVDD*3	Output
15	SWCLK	Input	16	Reserve	
17	SWDIO	Input/Output	18	Reserve	
19	Reserve		20	Reserve	
21	Reserve		22	Reserve	
23	Reserve		24	Reserve	
25	Reserve		26	Reserve	
27	Reserve		28	Reserve	
29	Reserve		30	Reserve	
31	Reserve		32	Reserve	
33	Reserve		34	Reserve	
35	Reserve		36	Reserve	
37	Reserve		38	Reserve	

Target connection reference diagram



*1: The target system side is taken as reference for Input/output. *2: SRST is an open drain output signal.

Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit. Connect VCC to a power supply that is less than 5V and matches the circuit of the target system.

31 Not used by our debugger; leave it as NC.
*4: If the SWV(Serial Wire Viewer) is not used for debugging or the CPU does

not support the SWV, do not connect anything to the SWO signal. *5: Connect to the I/O power supply of the CPU SWD signal.

This interface does not use TRST. If the target CPU has a TRST pin, connect a pull up resistor of 10K ohm.
 Keep the length of wirings from CPU to the target connector as short as possible. Otherwise, it could contribute to malfunction.
 When using Trace interface, refer <u>chw585_p4_etmtrace_if.pdf</u>.



Reference : RZ/A and RZ/T series /SRST, /TRST reference diagram

It may be required to control the $\overline{\text{RES}}$ and $\overline{\text{TRST}}$ CPU pins so that they are in low state at power on. Refer the CPU datasheet for details.

About Optional Conversion Probes

In addition to the conversion probe included in the PALMiCE4 standard set, we offer various optional conversion probes that can be used to connect to various target interfaces.

About Optional Conversion Probes

				●=Supp	ported /=N	ot supported
Draduat name	PALMiCE4 Model-J			PALMiCE4 Model-T		
Product name	ARM64	ARM	СМ	ARM64	ARM	СМ
ADP-ARM-MIL20-MS20 (CAP2R)	•	•	•	•	•	•
ADP-ARM-TI (CAP0E)	•	•	•	•	•	•
ADP-ISO-MIL20-MIL20 (CAP3F)	•	•	•			
ADP-JTAG20-ETM (CAP06)	•	•	•			
ADP-P4-MIC38-10HP (CAP3H)				•	•	•
ADP-P4-MIC38-20HP (CAP3K)				●	•	•
ADP-P4-MIC38-20HP-5V (CAP3E)				•	•	•
ADP-P4-MIC38-MIL20 (CAP3G)				●	•	●
PRB-MIL20-FLY6SWD (CP02J)	●	•		●	•	●
PRB-XIL-MIL20-2M14 (CAP3M)		•		●	•	
SWJ-PRB-MIL20-10HP (CP019)	●	•	•	●	•	●
SWJ-PRB-MIL20-20HP (CP01A)		•	•		•	●

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

SWJ-PRB-MIL20-10HP (CP019)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

SWJ-PRB-MIL20-10HP-E is a conversion probe for connecting Computex-made debugger^{*2} with 20-pin MIL connector^{*1} to 10-pin half-pitch (1.27mm) connector on the target system. The specifications of the connector on the target system are based on Serial Wire and JTAG specifications.



*1: 20-pin 2.54mm-pitch connector that supports JTAG interface.
*2: Please contact us for details on compatible products.

Outer shape and dimensional drawing of SWJ-PRB-MIL20-10HP



Connection



Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

Note

The direction of connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

10-pin connector on the target system side		10-pin connector on the target system side	
Pin No.	Signal	Pin No.	Signal
1	VTref	2	TMS/SWDIO
3	GND	4	TCK/SWCLK
5	GND	6	TDO/SWO
7	KEY	8	TDI
9	GND	10	SRST

SWJ-PRB-MIL20-20HP (CP01A)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

SWJ-PRB-MIL20-20HP-E is a conversion probe for connecting Computex-made debugger^{*2}with 20-pin MIL connector^{*1}to 20-pin half-pitch (1.27mm) connector on the target system. The specifications of the connector on the target system are based on Serial Wire and JTAG specifications.



*1: 20-pin 2.54mm-pitch connector that supports JTAG interface.
*2: Please contact us for details on compatible products.

Outer shape and dimensional drawing of SWJ-PRB-MIL20-20HP



Connection



Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

Table of connection wirings

20-pin connector on the target system side		20-pin connector on the target system side		
Pin No.	Signal	Pin No.	Signal	
1	VTref	2	TMS/SWDIO	
3	GND	4	TCK/SWCLK	
5	GND	6	TDO/SWO	
7	KEY	8	TDI	
9	GND	10	SRST	
11	GND ^{*3}	12	N.C. (TraceCLK/RTCK)	
13	GND ^{*3}	14	N.C. (TraceD0/SWO)	
15	GND	16	TRST (TraceD1/TRST)	
17	GND	18	N.C. (TraceD2)	
19	GND	20	N.C. (TraceD3)	

*3 : This pin may be assigned as the power supply pin on some target systems, In this product this is the GND pin. Make sure that you do not connect it to the power supply line (it can be left unconnected).

If pins 11 and 13 are assigned as power supply pins for the target system

ADP-20HP-20HP-1113NC

If pins 11 and 13 are assigned as power supply pins, connect the "ADP-20HP-20HP-1113NC" supplied with this product.

Outer shape and dimensional drawing of ADP-20HP-20HP-1113NC



Connection



Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

ADP-JTAG20-ETM (CAP06)

% The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

ADP JTAG-ETM is a conversion adapter for connecting Computex-made debugger with 20-pin JTAG connector to 38-pin ETM connector on the target system.



Outer shape and dimensional drawing of ADP-JTAG20-ETM



Connection



Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

20-pin connector on the target system side		20-pin connector on the target system side	
Pin No.	Signal	Pin No.	Signal
1	N.C.	2	N.C.
3	N.C.	4	N.C.
5	GND	6	N.C.
7	DBGRQ	8	DBGACK
9	SRST	10	N.C.
11	TDO	12	VTref
13	RTCK	14	Reserve
15	TCK	16	N.C.
17	TMS	18	N.C.
19	TDI	20	N.C.
21	TRST	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	N.C.
27	N.C.	28	N.C.
29	N.C.	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	N.C.
35	N.C.	36	N.C.
37	N.C.	38	N.C.

ADP-ARM-TI (CAP0E)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

ADP ARM-TI is a conversion adapter for connecting Computex-made debugger*1 with 20-pin JTAG connector to 14-pin MIL connector (TI-custom) on the target system.



*1 : Please contact us for details on compatible products.



Connection



Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

14-pin MIL connector (TI-custom)				
Pin No.	Signal	Pin No.	Signal	
1	TMS	2	TRST	
3	TDI	4	GND	
5	VTref	6	GND	
7	TDO	8	GND	
9	RTCK	10	GND	
11	TCK	12	GND	
13	N.C.	14	N.C.	

20-pin JTAG connector					
Pin No.	Signal	Pin No.	Signal		
1	VTref	2	N.C.		
3	TRST	4	GND		
5	TDI	6	GND		
7	TMS	8	GND		
9	TCK	10	GND		
11	RTCK	12	GND		
13	TDO	14	GND		
15	SRST	16	GND		
17	N.C.	18	GND		
19	N.C.	20	GND		



ADP-ARM-MIL20-MS20 (CAP2R)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

The ADP-ARM-MIL20-MS20 is a conversion adapter for connecting our debugger equipped with a 20-pin JTAG connector to the 20-pin MICRO SOCKET debug interface connector provided on a Texas Instruments target board.



Pitch specification of the MICRO SOCKET is as follows.

Outer shape and dimensional drawing of ADP-ARM-MIL20-MS20



Connection



Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

20-pin MIC on the	D-pin MICRO SOCKET connector on the target system side (① in Fig.) Target probe on PALMiCE JTAG200 side Pin No. (20-pin MICRO SOCKET on the target system (① in Fig.)		CRO SOCKET connector target system side (① in Fig.)	Target probe on PALMiCE JTAG200 side Pin No.	
Pin No.	Signal	(② in Fig.)	Pin No.	Signal	(② in Fig.)
1	TMS	7	2	TRST	3
3	TDI	5	4	N.C.	N.C.
5	VCC	1	6	N.C.	N.C.
7	TDO	13	8	GND	GND
9	RTCK	11	10	GND	GND
11	ТСК	9	12	GND	GND
13	EMU0	17	14	EMU1	19
15	SRST	15	16	GND	GND
17	N.C.	N.C.	18	N.C.	N.C.
19	N.C.	N.C.	20	GND	GND

ADP-P4-MIC38-20HP (CAP3K)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

The ADP-P4-MIC38-20HP is a conversion adapter for connecting our PALMiCE4 (Model-T) to the 20-pin 1.27mm pitch connector on the target system. This applies to both SWD and JTAG interfaces. Connect the Mictor probe (P4-PRB-KE68-MIC38) that comes with the PALMiCE4 (Model-T) to the 38-pin Mictor connector on this adapter. Then, connect the adapter's 20-pin 1.27mm pitch connector to the target system.



Outer shape and dimensional drawing of ADP-P4-MIC38-20HP



Connection



Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

Switch

Both JTAG/SWD interface and JTAG/SWD interface + Trace are supported. Set the use with the switch on the conversion adapter.

T⇔J	Switch settings	Explanation		
	т	Enable JTAG/SWD interface + Trace		
	J	Enable JTAG interface that uses RTCK, TRST signals		

20-pin connector on the target system side		20-pin connector on the target system side	
Pin No.	Signal	Pin No.	Signal
1	VTref	2	TMS/SWDIO
3	GND	4	TCK/SWCLK
5	GND	6	TDO/SWO
7	[KEY]	8	TDI
9	GND	10	SRST
11	GND	12	TRC_CK
13	GND	14	TRC_D0/RTCK
15	GND	16	TRC_D1/TRST
17	GND	18	TRC_D2
19	GND	20	TRC_D3

ADP-P4-MIC38-10HP (CAP3H)

% The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

The ADP-P4-MIC38-10HP is a conversion adapter for connecting our PALMiCE4 (Model-T) to the 10-pin 1.27mm pitch connector on the target system. This applies to both SWD and JTAG interfaces. Connect the Mictor probe (P4-PRB-KE68-MIC38) that comes with the PALMiCE4 (Model-T) to the 38-pin Mictor connector on this adapter. Then, connect the adapter's 10-pin 1.27mm pitch connector to the target system.



Outer shape and dimensional drawing of ADP-P4-MIC38-10HP



Connection



Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

10-pin 1.27mm-pitch connecter on the target system side		PALMiCE4 (Model-T) Mictor probe 38-pin Mictor connector	10-pin 1.27mm-pitch connecter on the target system side		PALMiCE4 (Model-T) Mictor probe 38-pin Mictor connector
Pin No.	Signal	Pin No.	Pin No. Pin No.		Signal
1	Vtref	12	2	TMS/SWDIO	17
3	GND	GND	4	TCK/SWCLK	15
5	GND	GND	6	TDO/SWO	11
7	Key	NC	8	TDI	19
9	GND	Reserve	10	SRST	9

1

PRB-XIL-MIL20-2M14 (CAP3M)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

PRB-XIL-MIL20-2M14 is a conversion probe for connecting Computex-made debugger^{*2}with 20-pin MIL connector^{*1}to 14-pin pitch (2mm) connector on the target system.

The specification of the connector on the target system are based on JTAG specification.

1

*1: 20-pin 2.54mm-pitch connector that supports JTAG interface. *2: PALMiCE4 Model-J、PALMiCE4 Model-T

Outer shape and dimensional drawing of PRB-XIL-MIL20-2M14



* About Compatible Connectors

Please refer to the target interface connector description in the AMD Xilinx "Platform Cable USB II" documentation. Example of compatible connector: Molex 87832-1420



Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

14-pin connector on the target system side		14-pin connector on the target system side	
Pin No.	Signal	Pin No.	Signal
1	GND	2	Vref
3	GND	4	TMS
5	GND	6	TCK
7	GND	8	TDO
9	GND	10	TDI
11	GND	12	N.C.
13	GND	14	SRST

PRB-MIL20-FLY6SWD (CP02J)

% The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

PRB-MIL20-FLY6SWD is a conversion probe for connecting our JTAG emulator to the CPU debug interface on the target system.





Connecting to STMicroelectronics STM32 NUCLEO

This section explains how to connect to STMicroelectronics STM32 NUCLEO development board. The STM32 NUCLEO board comes in three variants depending on the number of MCU pins, namely NUCLEO-32, NUCLEO-64 and NUCLEO-144.

In this example, NUCLEO-64 STM32L452 board is used as reference. To connect to NUCLEO-32 and NUCLEO-144 NUCLEO boards, refer to the relevant board documentation.

Connection



Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

Note

STM32 NUCLEO ST-LINK may issue a NRST signal periodically depending on the firmware version. If this happens, upgrade the ST-LINK firmware. Refer to STMicroelectronics website For the latest firmware information.

Table of connection wirings

The connection table between PRB-MIL20-FLY6SWD and STM32 NUCLEO-64 board STM32L452 is shown below. The STM32L452 has two types of boards, the STM32L452RE-P and the STM32L452RE.

PRB-MIL20-FLY6SWD		Connector point		
Signal name	Cable color	STM32L452RE-P	STM32L452RE	
VTref	Red	CN5-5 (VDD)	CN7-5 (VDD)	
GND	Black	CN3-3	CN4-3	
SWDIO	Grey	CN3-4	CN4-4	
SWCLK	Grey	CN3-2	CN4-2	
SWO	Grey	CN3-6	CN4-6	
SRST	Grev	CN3-5	CN4-5	

CN numbers for STM32L452 may be different for other NUCLEO boards.

Short CN2 1-2 and 3-4 pins on STM32L452RE-P and STM32L452RE board with jumper connectors.

ADP-P4-MIC38-MIL20 (CAP3G)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

The ADP-P4-MIC38-MIL20 is a conversion adapter for connecting our PALMiCE4 (Model-T) to the 20-pin 2.54mm pitch connector on the target system. This applies to both SWD and JTAG interfaces. Connect the Mictor probe (P4-PRB-KE68-MIC38) that comes with the PALMiCE4 (Model-T) to the 38-pin Mictor connector on this adapter. Then, connect the JTAG cable (JTAG-CB-MIL20-MIL20) that comes with PALMiCE4 (Model-T) to the 20-pin 2.54mm pitch connector of this adapter and connect the JTAG cable to the target system.



Outer shape and dimensional drawing of ADP-P4-MIC38-MIL20



Connection



Note

connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

Note

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

20-pin 2.54mm-pitch connecter on the target system side		PALMiCE4 (Model-T) Mictor probe 38-pin Mictor connector	20-pin 2.54mm-pitch connecter on the target system side		PALMiCE4 (Model-T) Mictor probe 38-pin Mictor connector
Pin No.	Signal	Pin No.	Pin No.	Signal	Pin No.
1	Vtref	12	2	TVDD	NC
3	TRST	21	4	GND	GND
5	TDI	19	6	GND	GND
7	TMS/SWDIO	17	8	GND	GND
9	TCK/SWCLK	15	10	GND	GND
11	RTCK	13	12	GND	GND
13	TDO/SWO	11	14	GND	GND
15	SRST	9	16	GND	GND
17	DBGRQ	7	18	GND	GND
19	DBGACK	8	20	GND	100ΩPull-down

ADP-ISO-MIL20-MIL20 (CAP3F)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

ADP-ISO-MIL20-MIL20 is an isolation adapter that electrically separates the PALMiCE4 Model-J unit from the target system.



Outer shape and dimensional drawing of ADP-ISO-MIL20-MIL20



Connection



Note

Ensure that each connector is connected in the right direction. When connecting, make sure to turn off the power of the PALMiCE4 unit and the target system beforehand.

Pin No.	Signal	Input/Output	Pin No.	Signal	Input/Output
1	VTref	Output	2	N.C.	-
3	TRST	Input	4	GND	-
5	TDI	Input	6	GND	-
7	TMS/SWDIO	Input / (Input/Output)	8	GND	-
9	TCK/SWCLK	Input	10	GND	-
11	N.C.	-	12	GND	-
13	TDO/SWO	Output	14	GND	-
15	SRST	Input	16	GND	-
17	N.C.	-	18	N.C.	-
19	N.C.	-	20	N.C.	-

Signal table on the target system side

Note

- 2. Input/Output is indicated with respect to the target system side.
- 3. The signal names and Input/Output within () are for SWD interface.

^{1.} These are partially different from the PALMiCE4 target interface technical documentation.

Target interface electrical characteristics

Current consumption	IDD (max)		20mA
		VTref = 1.8V	0.7V
	VIL (max)	VTref = 2.25V~5.5V	0.8V
input voitage level	VIH (min)	VTref = 1.8V	VTref × 0.75V
		VTref = 2.25V~5.5V	VTref × 0.7V
Outrast valtaria laval	VOL (max)		0.4V
Output voltage level	VOH (min)		VTref – 0.4V
Dreneration dalow		VTref = 1.8V	10nS~11nS
Propagation delay	IPLH/IPHL(Iyp)	VTref = 2.25V~5.5V	7nS~8nS

Note

- 1. This product consumes more power from the target system than VTref.
- 2. If the operation becomes unstable due to the propagation delay time of this product, lower the JTAG clock on CSIDE under Target system settings.

When Trace signal is 5V

ADP-P4-MIC38-20HP-5V (CAP3E)

%The code in parentheses after the product name is the product code. Please use it when looking at the price list on our website.

The ADP-P4-MIC38-20HP-5V is a Mictor conversion probe used with the PALMiCE4 Model-T that supports trace signal of 3.0~5.5V. The JTAG / SWD signal is compatible with 1.65~5.5V. If JTAG debug interface is used, this probe cannot be used on target systems that require $\overline{\text{TRST}}$ or RTCK signals.



Outer shape and dimensional drawing of ADP-P4-MIC38-20HP-5V



Note

The Mictor conversion probe-20P (Product name: ADP-P4-MIC38-20HP) included in the standard set supports trace signals of 3.6V or less.

Note

Note that ADP-P4-MIC38-20HP-5V (this product) and ADP-P4-MIC38-20HP (standard set product) are similar in shape. They can be distinguished via the product name sticker (on the body) and by checking their external appearance.



Connection 20-pin 1.27mm-pitch connector ADP-P4-MIC38-20HP Mictor probe

Note

Target system

The direction of connection is predetermined for each connector. In establishing connection, pay attention to its orientation.

T-PWR STS RUN PWR

PALMICE 4

utex PALMiCE4 main unit

When connecting this product, do so after turning OFF the power of the debugger main unit and the target system.

Signal table on the target system side

Pin No.	Signal	Input/Output	Pin No.	Signal	Input/Output
1	VTref	Output	2	TMS/SWDIO	Input/Output
3	GND	-	4	TCK/SWCLK	Input
5	GND	-	6	TDO/SWO	Output
7	KEY	-	8	TDI	Input
9	GND	-	10	SRST	Input
11	GND	-	12	TRC_CLK	Output
13	GND	-	14	TRC_D0	Output
15	GND	-	16	TRC_D1	Output
17	GND	-	18	TRC_D2	Output
19	GND	-	20	TRC_D3	Output

Note

1. These are partially different from the PALMiCE4 target interface technical documentation. 2.Input/Output is indicated with respect to the target system side.

Target interface electrical characteristics

	VIL (max)	0.8V
Input voltage level	VIH (min)	2.0V

Note

1. For signal specifications other than trace signals, refer to "PALMiCE4 Hardware Manual".

2. When this product is used, CSIDE settings for [ETM signal conditions]-[EMT reference voltage] is invalid.

Technical Information on JTAG / SWD / SWV / ETM ARM-related Target Interface (12th Edition)

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PALMiCE4

Hardware Manual

(11th Edition)

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Precautions for use

Read the following thoroughly before attempting to use the product.

- In the event of exporting the product (including taking it outside of Japan) or supplying the software to third parties not residing in Japan, make sure that all procedures as stipulated by the Foreign Exchange and Foreign Trade Act are strictly observed.
- The product, the product manual and the software may not be used or reproduced in whole or in part without prior permission.
- Product details and specifications are subject to modification without prior notice for the purpose of improving reliability, functionality and design.
- Note that although a great deal of care has been taken in manufacturing the product, the company does not guarantee the results of its use.
- Do not install the product in locations subject to excessive amounts of water, humidity, dust, oily vapor, etc., as it may result in the outbreak of fire, malfunctions or electric shock. Make sure that the correct power supply and voltage as listed is used.
- All copyrights pertaining to CSIDE are the sole property of Computex Co., Ltd.
- CSIDE, PALMICE, and COMPUTEX are registered trademarks of Computex Co., Ltd., Japan.
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Chapter 1 Getting Started

1.1 Introduction

This document explains PALMiCE4 hardware specifications. Refer the User's manual for details on software specifications.

PALMiCE4 ARM is available in two models. **Model-J** that is specialized for JTAG debugging, and **Model-T** which is a highly functional model that incorporates Trace function along with JTAG debugging. Both models have a palm-sized compact design. USB is used for interfacing with a PC, so no power supply is needed (Vbus compatible^{*1}). This makes PALMiCE4 the ideal debugging tool and easy to carry around with a laptop while debugging or on a business trip.

- Model-J : JTAG debugger
- Model-T : JTAG debugger with trace function

As the next advanced version of PALMiCE3, PALMiCE4 series come with a new Real-time monitor function. In addition, Model-T is equipped with Trace function that provides a more complete debugging environment.

Main features of PALMiCE4 ARM:

[Model-J / Model-T common features]

- Supports almost all ARM core processors available in the market
- JTAG / SWD / SWV debug interfaces supported
- Supports CoreSight on-chip debugging/tracing technology
- Real-time monitor function
- Supports both internal and external flash memory
- USB 3.0 compatible, supports super speed, high speed, full speed
- No external power supply needed(Vbus compatible^{*1})
- Instant connection to the host PC and the target board
- Palm-sized, light, and compact body

[Model-T specific features]

- Built-in 4GB trace memory
- Supported debug interface: JTAG / SWD / SWV / ETM / PTM
- *1: Refer "2.1.1 About Vbus" for more information

NOTE Real-time monitor function al

Real-time monitor function allows reading and modifying memory contents and performing debugging without stopping CPU execution. The real-time values of variables at regular intervals are displayed on a graph.

1.2 Product Composition 1.2.1 Model-J

•PALMiCE4 Model-J unit ······x 1	T-PWR STS R.N PWR
	PALMICE 4
	Computex
•JTAG cable (20-pin 2.54mm-pitch connector) (Approx. 17cm) [J-1]	
•External probe······x 1 "P4-EXPRB-3CP"	
•USB cable	

•Software "CSIDE" (including a set of manuals) *Downloadable

* Refer to the "Packing List" (paper) included with the product for available software.

* For details on downloading, please refer to "1.3 About software download".



1.2.2 Model-T •PALMiCE4 Model-T unit ······ x 1 T-PWR STS RUN PWR PALMICE 4 **Compute**x •Mictor probe (38-pin Mictor connector) (Approx. 46.5cm) [T-1] ·······x 1 "P4-PRB-KE68-MIC38" "P4-EXPRB-3CP" "P4-ANPRB-5CP" •USB cable ······ x 1 (USB3.0/A-microB/2m) •AC adapter ····· x 1 (5V 2A)

•Software "CSIDE" (including a set of manuals) *Downloadable

* Refer to the "Packing List" (paper) included with the product for available software.

* For details on downloading, please refer to "1.3 About software download"



In case of Model-T, in addition to the Mictor probe, a probe matching the interface specifications of the target system is available.

•JTAG cable (20-pin 2.54mm-pitch connector) (Approx. 17cm) [T-2] ······x 1 "JTAG-CB-MIL20-MIL20"



•JTAG conversion probe (20-pin 2.54mm-pitch connector) (Approx. 14cm) [T-3] ·· x 1 "ADP-P4-20HP-MIL20"





1.2.3 About Optional Products

PALMiCE4 offers a variety of optional products for use with a wide range of targets and systems. For details on the combination of optional products and usage configurations, please refer to the "ARM-related JTAG / SWD / SWV / ETM Target Interface Technical Documents" on our website (<u>https://www.computex.co.jp/</u>).

1.3 About software download

Please download and install the software included in this product from the following website.

■ Software download site : https://www.computex.co.jp/support/download/cd/

For download details, please refer to the download instructions PDF on the download site.

In addition to the download procedure, these instructions also describe what is required to download the software and the relationship between the software and the license.

1.4 Product combination

The combination depends on the connectors and debug I/Fs available on the target system.

The explanation is given for each model.

By using a conversion probe (optional product), connections other than those described here are also possible.

For details on the combination of optional products and usage configurations, please refer to the "ARM-related JTAG / SWD / SWV / ETM Target Interface Technical Documents" on our website (<u>https://www.computex.co.jp/</u>).

1.4.1 Overview

Model-J

Тгасе		Target system			Required probe	Reference
Debug I/F	(ETM, SWV) support	On-board connector	Debug I/F	Trace (ETM、SWV) support	cable *1	case *2
JTAG		20-pin 2.54mm-pitch connector	JTAG		【J-1】	1
JTAG		20-pin 1.27mm-pitch connector	JTAG			
JTAG		10-pin 1.27mm-pitch connector	JTAG		Supported by conversion	n probe
JTAG		14-pin 2mm-pitch connector	JTAG		 (optional product) *3 	
SWD		20-pin 2.54mm-pitch connector	SWD		[J-1]	1
SWD		20-pin 1.27mm-pitch connector	SWD		Supported by conversion probe	
SWD		10-pin 1.27mm-pitch connector SWD (optional produc		(optional product) *3		

*1 : Model numbers are linked to the ones listed in "1.2 Product Composition".

*2 : Numbers shown are reference cases described in "1.5.1 Model-J".

*3 : A conversion probe (optional product) is required separately. For details, please refer to "ARM-related JTAG / SWD / SWV / ETM Target Interface Technical Document" on our home page.

	Trace Target system			Required probe	Reference	
Debug I/F	(ETM, SWV) support	On-board connector	Debug I/F	Trace (ETM、SWV) support	cable *1	case *2
JTAG	0	38-pin Mictor connector	JTAG	0	[T-1]	2
		38-pin Mictor connector		0		0
JTAG	0	20-pin 2.54mm-pitch connector	JTAG		[T-1]+[T-2]+[T-3]	3
					[T-1]+[T-4]	4
JTAG O		20-pin 1.27mm-pitch connector	JTAG	0	Supported by conversion probe	
JTAG		10-pin 1.27mm-pitch connector	JTAG		(optional product) *3	
JTAG		20-pin 2.54mm-pitch connector	JTAG		[T-1]+[T-2]+[T-3]	5
JTAG		14-pin 2mm-pitch connector	JTAG		Supported by conversion probe (optional product) *3	
					[T-1]+[T-4]	4
SWD	0	20-pin 1.27mm-pitch connector	nector SWD O	Supported by conversion probe		
SWD		10-pin 1.27mm-pitch connector	SWD		(optional product) *3	
SWD		20-pin 2.54mm-pitch connector	SWD		[T-1]+[T-2]+[T-3]	5

Model-T

***1** : Model numbers are shown in "1.2 Product Composition".

*2 : Numbers shown are reference cases described in "1.5.2 Model-T".

*3 : A conversion probe (optional product) is required separately. For details, please refer to "ARM-related JTAG / SWD / SWV / ETM Target Interface Technical Document" on our home page.



1.5 Product combination depiction

This section describes a few combinations that are possible for products listed in "1.2 Product Composition".

For information about conversion probes (optional products), please refer to "ARM Related JTAG / SWD / SWV / ETM Target Interface Technical Document" on our home page.

The combination used is linked to the list in "1.4 Product combination1.4 Product combination". Please refer to it as well.

1.5.1 Model-J

Reference case①





1.5.2 Model-T

Reference case2

Debug interface	Trace(ETM、SWV)	Target system connector
JTAG or SWD	Supported	38-pin Mictor connector



Reference case3

Debug interface	Trace(ETM、SWV)	Target system connector	
	Supported	38-pin Mictor connector (Trace) 20-pin 2.54mm-pitch connector (JTAG)	
JIAG OF SWD	Supported		



Reference case④

Debug interface	Trace(ETM、SWV)	Target system connector
JTAG or SWD	Supported	20-pin 1.27mm-pitch connector



Reference case5

Debug interface	Trace(ETM、SWV)	Target system connector
JTAG or SWD	Not supported	20-pin 2.54mm-pitch connector





Chapter 2 PALMiCE4 Hardware Specifications

2.1 PALMiCE4 specifications

The specifications of Model-J and Model-T are as sown in the table below:

	ltem	Model-J specifications	Model-T specifications	
Supj debi	ported ug interface	JTAG / SWD / SWV	JTAG / SWD / SWV / ETM / PTM	
Т	Connector specifications	20-pin complying to ARM specification	38-pin complying to ARM specification	
arget int	Target system side connector specifications	20-pin 2.54mm-pitch connector	AMP-made 38-pin Mictor connector 2-5767004-2 / 5767054-1 / 5767061-1	
erface ^{*1}	Voltage	JTAG : 1.65V - 5.5V (depends on target)	JTAG : 1.65V - 5.5V (depends on target) Trace : 1.0V - 3.6V (depends on target) / 3.0V - 5.5V (depends on target) *3 Analyzer: 1.65V - 5.5V	
Trace memory -		-	4-GByte (512M frame × 64-bit)	
Trace size - 1-bit / 2-bit / 4-bit / 8-bit		1-bit / 2-bit / 4-bit / 8-bit		
Trac	e clock	-	Max200MHz (single-edge, dual-edge)	
Trac	e timestamp	-	Yes (1us or 50ns clock)	
LED		T-PWR / STS / RUN / PWR		
Outside dimensions		108.40mm(W)×81.00mm(D)×28.45mm(H) * Excluding the connector		
Operating environment Open		Operating temperature: 5°C to 40°C Operating humidity level: 35% to 85%RH		
USB host interface		USB3.0 microB connector		
Power supply		USB Vbus	USB Vbus *2	
Curr	ent consumption	DC5V ±5% Approx. 400mA max	DC5V ±5% Approx. 700mA max	
Wei	ght	Approx. 180g		

*1 : The following connectors can be used with the included conversion adapter and optional products as per requirement (some features are not available as indicated):

•20-pin 2.54mm-pitch connector (*Trace cannot be used)

·20-pin 1.27mm-pitch connector (*Up to 4 bits can be used during Trace in Model-T)

•10-pin 1.27mm-pitch connector (*Trace cannot be used)

*2 : Refer "2.1.1 About Vbus" for details

*3 : When using Mictor conversion probe-20P-5V(ADP-P4-MIC38-20HP-5V), Trace voltage will be (3.0V to 5.5V).

2.1.1 About Vbus

USB devices are classified into "High-power devices" and "Low-power devices", depending on the current required for the device to operate.

Low-power devices require a power supply of 100mA or less.

High-power devices require a maximum power supply of 500mA in case of USB2.0 and 900mA in case of USB3.0.

PALMiCE4 is a high-power device.

PALMiCE4 will not work with USB hubs that only support low-power devices.

For example, some USB hubs on USB keyboards support only low-power devices. PALMiCE4 will not work if connected to such hubs.

If you are using a PC that does not support USB3.0 specification, the Vbus current will be insufficient for PALMiCE4 Model-T. In such cases, connect the provided AC adapter.

Refer to the manual of the PC or USB hub to check if high-power devices are supported and if the USB port is USB2.0 or USB3.0.

2.2 PALMiCE4 - parts explained

2.2.1 PALMiCE4 unit

Model-J exterior appearance



Model-T exterior appearance



[1]	T-PWR LED	Green when the target system power is detected.	
[2]	STS LED	Green when USB connection with the host PC is successful.	
		Blinks when there is no response while waiting for driver authentication etc.	
[3]	RUN LED	Green when the user program is being executed.	
		Blinks when Trace data is captured in case of Model-T	
[4]	PWR LED	Green when PALMiCE4 is turned on.	
		In case of Model-J, power is supplied from the host PC USB Vbus. In case of	
		Model-T, power can be supplied from the AC adapter as well.	
[5]	Target side panel	In case of Model-J, refer "2.2.2 Model-J".	
		In case of Model-T, refer "2.2.3 Model-T".	
[6]	Host side panel	In case of Model-J, refer "2.2.2 Model-J".	
		In case of Model-T, refer "2.2.3 Model-T".	

2.2.2 Model-J





Target-side panel

Host-side panel

[1]	TARGET connector	The provided JTAG cable has to be connected here.
[2]	CRCN connector	Reserved for future use. Socket that will be used with CodeRecorder CR-200.
[3]	EXCN1 / EXCN2 connector	Socket where the provided external probe has to be connected.
		Refer "2.3.3 External probe [Model-J] [Model-T]" for details.
[4]	USB connector	Connect the included USB cable (USB3.0 microB specification) here.
[5]	Power switch	Power on/off PALMiCE4 via this switch. Power status can be confirmed by PWR
		LED.



2.2.4 Hardware revision

A sticker with the following information can be found under the PALMiCE4 unit.



Underside of PALMiCE4 unit

How to read revision sticker

The revision consists of a major version and a minor version.

On the sticker, the individual digit is the major version and the last blacked out alphabet is the minor version.

Example 1): Hardware revision 1-B

	А	в
1	С	D
Е	F	G
н	-	J
к	L	м
Ν	0	Р

In this example, the number is 1 and both A and B are shaded, but only B has to be considered. So, the hardware revision is **1-B**.

Example 2): Hardware revision 2-0

	А	в
2	С	D
Е	F	G
н	-	J
к	L	М
N	0	Ρ

In this example, the number is 2 and none of the alphabets are shaded. So, the hardware revision is **2-0**.

2.3 Probe and cables

This section describes the probes and cables that come with the standard set. The standard set name is shown next to the name of each probe. For example, "Mictor probe [Model-T]" can be interpreted as a Mictor probe for PALMiCE4 ARM (Model-T).





[1]	PALMiCE4 connector	This side of the probe has to be connected to the TARGET connector on the	
		PALMiCE4 Model-T unit.	
[2]	Target connector	38-pin Mictor connector that has to be connected to the target system.	
[3]	JTAG connector	This is where the JTAG conversion probe-20 [T-3] has to be connected when	
		connecting to a target system that has a JTAG signal connector separate from the	
		38-pin Mictor connector. Reference case ③ corresponds to such cases.	
[4]	ANCN connector	This is where the analyzer probe has to be connected. It is used to observe the state of	
		external signals.	
		Refer "2.3.4 Analyzer probe [Model-T]" for details.	
[5]	CRCN connector	Reserved for future use. This will be used with CodeRecorder CR-200.	



2.3.3 External probe [Model-J] [Model-T]

The external probe is used to synchronize with the target system. This probe is optional and can be disconnected when not in use. A single-pulse (negative logic) trigger is output on the TRGOUT line when the CPU trace "Break when trace memory is full" condition is met or when the event condition on the real-time monitor function is met. BRKIN input line is used to break the user program by an arbitrary external signal or to start the real-time monitor function.



TRGOUT signal is output at the following timing:



The internal circuit is as shown below. The input has to be LVTTL level. Make sure not to apply voltage exceeding the absolute maximum IC rating of $0.5V \sim 3.6V$. The circuit will fail otherwise.



NOTE

EXCN1 and EXCN2 connectors are for connecting the BRKIN input and TRGOUT output signals of PALMiCE4 to the target system. EXCN1 and EXCN2 are connected to the same lines internally, so <u>when using the external probe, connect it</u> <u>only one of them.</u> They are not two separate entities internally.

2.3.4 Analyzer probe [Model-T]

The analyzer probe is used to observe the state of the external signals along with trace data. This probe is optional and can be disconnected when not in use.

This probe is connected to the ANCN connector of the Mictor probe used with Model-T. Four external signals can be connected.



2.3.5 JTAG conversion probe [Model-T]

A target system with a 20-pin 2.54 mm pitch JTAG connector can be connected to PALMiCE4 Model-T via this conversion probe. This conversion probe has to be connected to the JTAG connector on the Mictor probe.

This side can has to be connected to JTAG connector of the Mictor probe.

While most target systems have JTAG signals and Trace signals on the same 38-pin Mictor connector, some may have separate connectors. Use this JTAG conversion probe to connect both the JTAG connector and the Trace connector. Reference case ③ corresponds to such cases.

2.3.6 Mictor conversion adapter-20P [Model-T]



[1]	38-pin Mictor connector	This side has to be to be connected to the Mictor probe.
[2]	Target connector	20-pin 1.27mm pitch connector that has to be connected to the target system.
[3]	Switch	Switch for switching between JTAG/SWD interface and JTAG/SWD interface +
		Trace.

A target system with a 20-pin 1.27 mm pitch connector can be connected to PALMiCE4 Model-T via this conversion probe. Both JTAG/SWD interface and JTAG/SWD interface + Trace are supported.

JTAG	Switch settings	Explanation
	TRC	Enable JTAG/SWD interface + Trace
	JTAG	Enable JTAG interface that uses RTCK, TRSTn signals

[2]

JTAG connector

Chapter 3 Target Interface Specifications

3.1 Introduction

This chapter explains the interface specifications for connecting PALMiCE4 to the target system.



The interface for connecting PALMiCE4 Model-J to the target system is described here.

3.2.1 Shape of the connector for debugger

The shape of the debugger connector (20-pin MIL connector) that is usually mounted on the target system is shown here.

(Top view on the target system)



(For detailed dimensions of the connector, refer to the documentations provided by the manufacturer)

3.2.2 Dimension of the JTAG cable

The dimension of JTAG cable for connecting PALMiCE4 Model-J to the target system is shown here.



(For detailed dimensions of the connector, refer to the documentations provided by the manufacturer)

3.2.3 Specifications of target interface signals

		Tarrat 1.8V	Target voltage × 0.35V	
	VIL(min) V	Target	3.3V	0.8V
Innut voltago loval		voitage	5.0V	Target voltage × 0.3V
input voltage level		Target voltage	1.8V	Target voltage × 0.65V
	VIH(max)		3.3V	2.0V
			5.0V	Target voltage × 0.7V
Output voltage level	ge level VOL VOH			0V ∼ 0.55V*
Output voltage level			2.4V [*] ~ Target voltage	

* Target voltage =3.3V IOL/IOH=±24mA reference value

3.2.4 The target interface on PALMiCE4 side

The target interface on PALMiCE4 side is described below.

The terminal/pin numbers and the target cable are specific to **PALMiCE4**. Make sure only to use the product cable supplied with the product.



Terminal No.	Remarks	Terminal No.	Remarks
1	5.5KΩ Pull-down	2	
3	22Ω Series	4	
5	22Ω Series	6	
7	22Ω Series 10KΩ Pull-up ^{*1}	8	
9	22Ω Series	10	
11	22Ω Series 100KΩ Pull-down	12	
13	22Ω Series 10KΩ Pull-up ^{*1}	14	
15	100Ω Series Open drain	16	
17	22Ω Series	18	
19	22Ω Series 100KΩ Pull-down	20	

*1 : Signals will be pulled up to the voltage level detected on VTref pin.

NOTE For Target connection reference diagram, refer to "Technical Information on JTAG ARM-related Target Interface" on our website (<u>http://www.computex.co.jp/eg/</u>).

3.3 Model-T specifications

The interface for connecting PALMiCE4 Model-T to the target system is described here.



The shape of connector (38-pin Mictor connector) for PALMiCE4 to be mounted on the target system is as follows.





Recommended connector: Manufacturer: AMP Model : Mictor connector 2-5767004-2 / 5767054-1 / 5767061-1

(For detailed dimensions of the connector, refer to the documentations provided by manufacturer)

During manufacturing/design, it is recommended to place the Mictor connector as close as possible to the CPU so that the wiring pattern length is minimized. While placing the JTAG connector, it is recommended to place it close to the Mictor connector. Also, the Grand Bus Leads of Mictor connector needs to be connected to GND.



3.3.2 Shape of the connector for debugger (20-pin 1.27mm-pitch connector)

The shape of connector (20-pin 1.27mm-pitch connector) for PALMiCE4 to be mounted on the target system is as follows.

(Top view on the target system)



Recommended connector: Manufacturer: Samtec, Inc. Model : FTSH-110-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentations provided by manufacturer)

During manufacturing/design, it is recommended to place the connector as close as possible to the CPU so that the wiring pattern length is minimized.

3.3.3 Dimensions of the Mictor probe

The dimensions of the provided Mictor probe are as indicated here.

Product name : P4-PRB-KE68-MIC38



Mictor connector



3.3.4 Dimensions of the ADP-P4-MIC38-20HP-CN adapter



- Make sure to check the position of Pin 1. Incorrect orientation may cause a malfunction.
- The ADP-P4-MIC38-20HP-CN adapter consists of the main unit and the extension adapter.
- Extension adapter prevents reverse insertion into the target system and the extension interferes when a connector with a key is installed.

If reverse insertion prevention key is not present, it can be removed.

(Do not discard it and keep it safe for future use) Extension adapter tip connector : FLE-110-01-G-DV

3.3.5 Specifications of the target interface signals

Signals other than Trace and Analyzer signals		Signals other	than Trace	and Analyzer	signals
---	--	---------------	------------	--------------	---------

	VIL(min)	Target 1.8V		Target voltage × 0.35V
		voltage	3.3V	0.8V
			5.0V	Target voltage × 0.3V
input voltage level	VIH(max)	Target	1.8V	Target voltage × 0.65V
			3.3V	2.0V
		voitage	5.0V	Target voltage × 0.7V
	VOL			0V - 0.55V*
Output voltage level	VOH			2.4V [*] - Target voltage

* Target voltage =3.3V IOL/IOH=±24mA reference value

Trace signal

Innut valtana laval	VIL(max)	Target voltage ÷ 2 - 0.1 (V)
input voltage level	VIH(min)	Target voltage ÷ 2 (V)

Analyzer signal

	VIL(max)	0.89V - 1.2V
input voltage level	VIH(min)	1.48V - 1.92V

3.3.6 38 Pin Mictor connector signal table

The target interface is described here.

Terminal No.	Remarks	Terminal No.	Remarks
1		2	
3		4	
5		6	
7	22Ω Series	8	22Ω Series 100KΩ Pull-down
9	100Ω Series Open drain	10	
11	22Ω Series 10KΩ Pull-up ^{*1}	12	5.5KΩ Pull-down
13	22Ω Series 100KΩ Pull-down	14	
15	22Ω Series	16	
17	22Ω Series 10KΩ Pull-up ^{*1}	18	
19	22Ω Series	20	
21	22Ω Series	22	
23		24	
25		26	
27		28	
29		30	
31		32	
33		34	
35		36	
37		38	

*1 : Signals will be pulled up to the voltage level detected on VTref pin.

NOTE

For Target connection reference diagram, refer to "Technical Information on JTAG ARM-related Target Interface" on our website (<u>http://www.computex.co.jp/eg/</u>).

3.3.7 20 Pin 1.27mm pitch connector signal table

The target interface is described here.

Terminal No.	Remarks	Terminal No.	Remarks
1	5.5KΩ Pull-down	2	22Ω Series 10KΩ Pull-up ^{*1}
3		4	22Ω Series
5		6	22Ω Series 10KΩ Pull-up ^{*1}
7		8	22Ω Series
9		10	100Ω Series Open drain
11		12	
13		14	
15		16	
17		18	
19		20	

*1: Signals will be pulled up to the voltage level detected on VTref pin.

NOTE

For Target connection reference diagram, refer to "Technical Information on JTAG ARM-related Target Interface" on our website (<u>http://www.computex.co.jp/eg/</u>).



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