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# Technical Information

## ARM-related

### JTAG / SWD / SWV / ETM Target Interfaces

Mar. 04, 2011  
Third Edition

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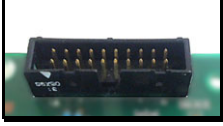
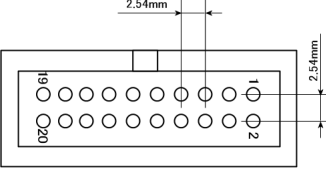
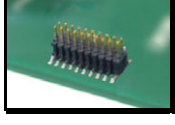
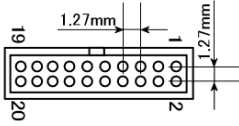
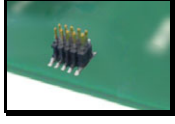
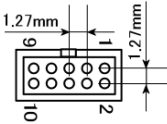
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## Document change history

First Edition	Sep. 11, 2009	Initial edition
Second Edition	Nov. 13, 2009	<ul style="list-style-type: none"> <li>• Added the descriptions on CPU core "ARM" and "PALMiCE3 ARM (JTAG200)" to Technical Information reference chart and Product purchase chart.</li> <li>• Corrected the Product purchase chart. Technical Information ④ and ⑥ correspond to PALMiCE3 CM3 (ETM200) only. However, PALMiCE3 CM3(ETM200) is a product to be released in the future.</li> <li>• Added the note on <math>\overline{\text{SRST}}</math> signal in respective signal tables. "<math>\overline{\text{SRST}}</math> signal is an open-collector output."</li> </ul>
Third Edition	Mar. 04, 2011	<ul style="list-style-type: none"> <li>• PALMiCE3 CM3(ETM200) has already been released (Dec. 2009). Deleted the following description: "To be released in the future."</li> <li>• "Supported connectors" Added graphic images of the connectors.</li> <li>• "Product purchase chart" Added graphic images of the optional products.</li> <li>• Added the note on <math>\overline{\text{SRST}}</math> signal in respective signal tables.</li> <li>• Changed the note on <math>\overline{\text{TRST}}</math> signal in respective signal tables.</li> <li>• Deleted CPU core options from Technical Information reference chart and Product purchase chart. For supported CPUs, refer to Product Summary of respective products up on our website.</li> <li>• Deleted the description of the case where ETM is not used and half-pitch (1.27mm) connector is used. When you use them, please contact us.</li> </ul>

## Supported connectors

(For detailed dimensions of the connectors, refer to the documentations by respective manufacturers of the connectors.)

<p><b>20-pin 2.54mm-pitch connector</b></p> 	 <p>(Top view on the target board)</p>	<p>Recommended connector                      Manufacturer: OMRON Corporation                      Model : XG4C-2031</p>
<p><b>20-pin 1.27mm-pitch connector</b></p> 	 <p>(Top view on the target board)</p>	<p>Recommended connector                      Manufacturer: Samtec, Inc.                      Model : FTSH-110-01-L-DV-K</p>
<p><b>10-pin 1.27mm-pitch connector</b></p> 	 <p>(Top view on the target board)</p>	<p>Recommended connector                      Manufacturer: Samtec, Inc.                      Model : FTSH-105-01-L-DV-K</p>

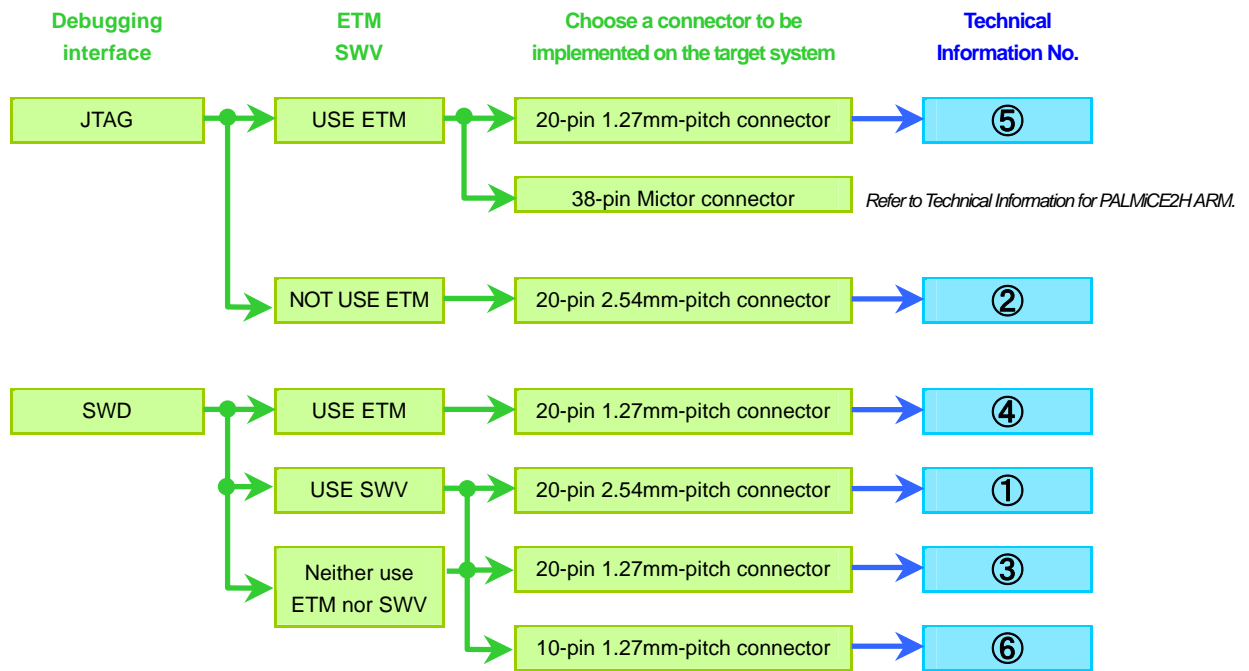
## Applicable products

This manual is applicable for the following products.

- PALMiCE3 ARM (JTAG200)
- PALMiCE3 CM3 (ETM200)
- J-STICK STM32
- J-STICK TX03
- J-STICK Stellaris

### Technical Information reference chart

Depending on the target interface you use, Technical Information you should refer to will be different. Based on the chart below, consult the applicable Technical Information.



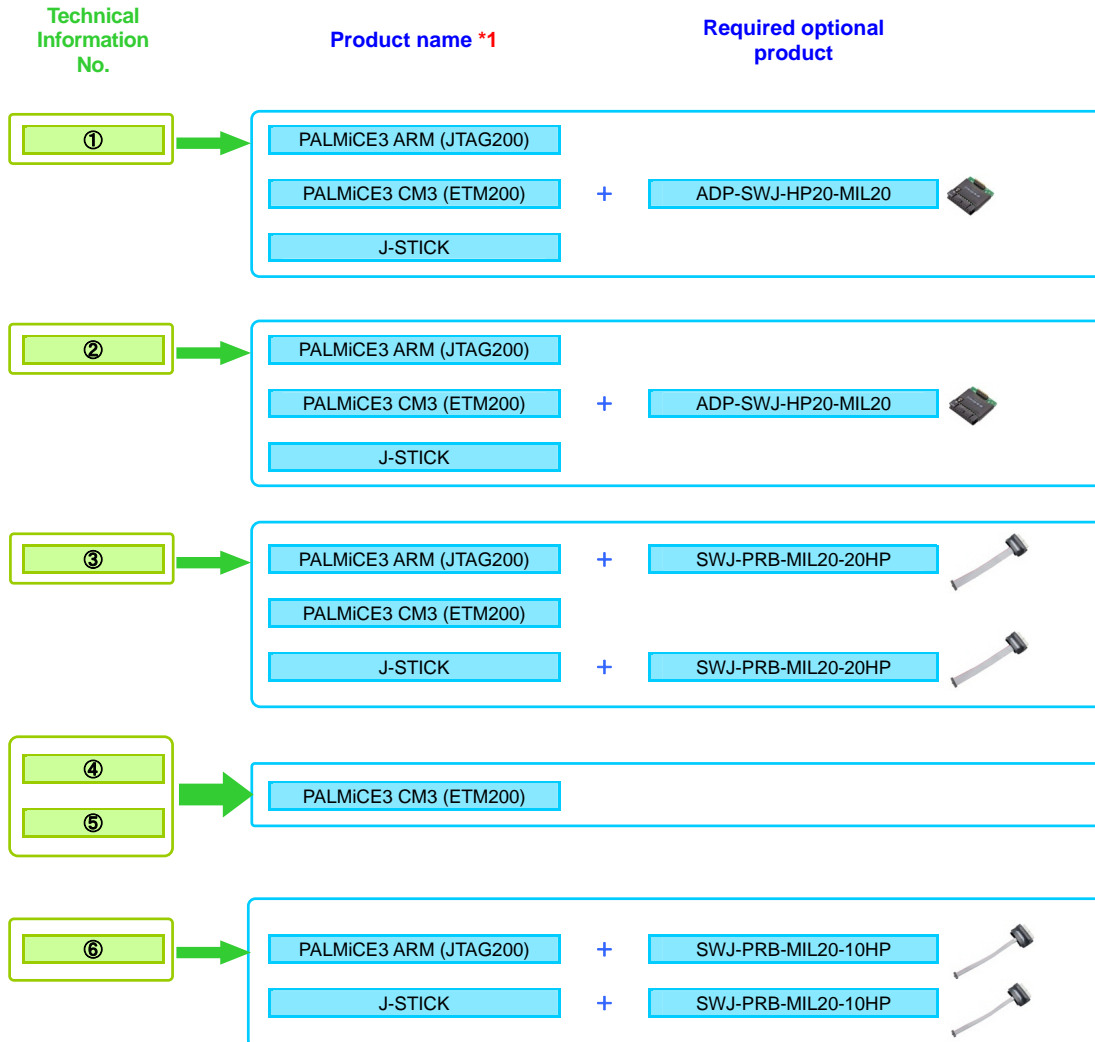
\* : Only those combinations available for selection are given. For other combinations, please contact us.

### Product purchase chart

Depending on the target interface you use, the composition of product and optional product you should purchase will differ.

Based on the Technical Information No. (See "Technical Information reference chart" on the previous page), choose the product.

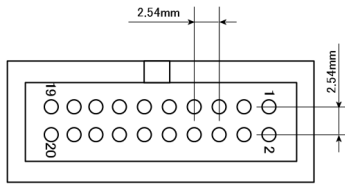
\* : Only those products available for selection are given.



\*1 : For CPUs supported in each product, refer to Product Summary of respective products up on our website.

## 20-pin 2.54mm-pitch connector

### Target connector specifications



(Top view on the target board)

Recommended connector  
 Manufacturer: OMRON Corporation  
 Model: XG4C-2031

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

## ① SWD interface

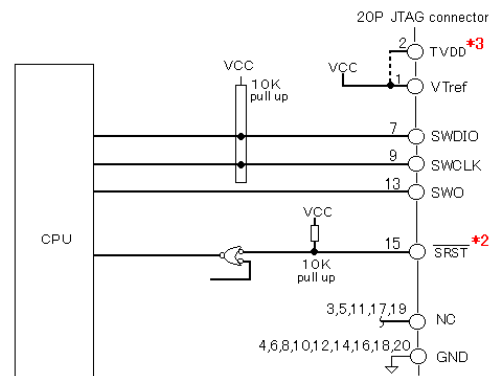
### Signals

Pin No.	Signal	Input/Output <sup>*1</sup>	Pin No.	Signal	Input/Output <sup>*1</sup>
1	VTref	Output	2	TVDD	Output
3	NC		4	GND	
5	NC		6	GND	
7	SWDIO	Input/Output	8	GND	
9	SWCLK	Input	10	GND	
11	NC		12	GND	
13	SWO	Output	14	GND	
15	SRST <sup>*2</sup>		16	GND	
17	NC		18	GND	
19	NC		20	GND	

- \*1: Input/output is based on the target system.
- \*2: SRST signal is an open-collector output. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
- \*3: The signal is not used by Computex-made debugger; it can be left unconnected.

- This interface does not use  $\overline{\text{TRST}}$ . If the target CPU presents a pin specifically for  $\overline{\text{TRST}}$ , pull it up with 10K ohmic value.
- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

### Target connection reference diagram



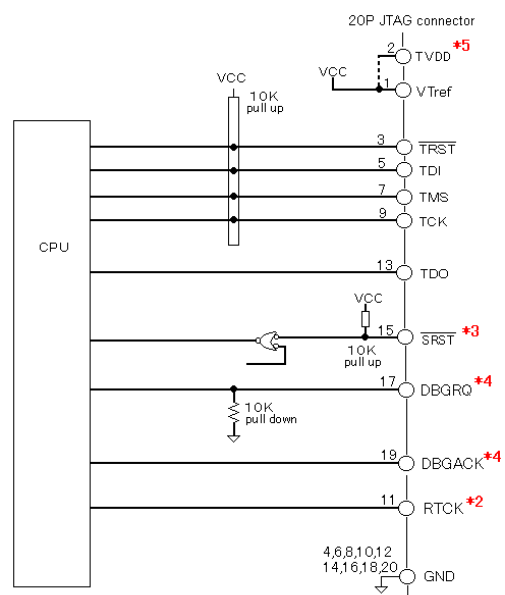
## ② JTAG interface

### Signals

Pin No.	Signal	Input/Output <sup>*1</sup>	Pin No.	Signal	Input/Output <sup>*1</sup>
1	VTref	Output	2	TVDD	Output
3	$\overline{\text{TRST}}$	Input	4	GND	
5	TDI	Input	6	GND	
7	TMS	Input	8	GND	
9	TCK	Input	10	GND	
11	RTCK <sup>*2</sup>	Output	12	GND	
13	TDO	Output	14	GND	
15	SRST <sup>*3</sup>	Input	16	GND	
17	DBGRO <sup>*4</sup>	Input	18	GND	
19	DBGACK <sup>*4</sup>	Output	20	GND	

- \*1: Input/output is based on the target system.
- \*2: If the CPU does not present the pin or if you do not use RTCK, leave it as N.C..
- \*3: SRST signal is an open-collector output. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.
- \*4: In the CPUs that do not present this signal, leave the pin unconnected in open state.
- \*5: The signal is not used by Computex-made debugger; it can be left unconnected.

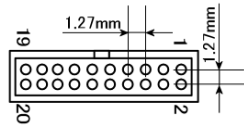
### Target connection reference diagram



- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

## 20-pin 1.27mm-pitch connector

### Target connector specifications



(Top view on the target board)

Recommended connector

Manufacturer: Samtec, Inc.

Model: FTSH-110-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

### 3 SWD interface

#### Signals

Pin No.	Signal	Input/Output <sup>*1</sup>	Pin No.	Signal	Input/Output <sup>*1</sup>
1	Vtref	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO	Output
7	Key <sup>*3</sup>		8	NC	
9	GND		10	SRST <sup>*2</sup>	Input
11	GND		12	NC	
13	GND		14	NC	
15	GND		16	NC	
17	GND		18	NC	
19	GND		20	NC	

\*1: Input/output is based on the target system.

\*2: SRST signal is an open-collector output.

Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.

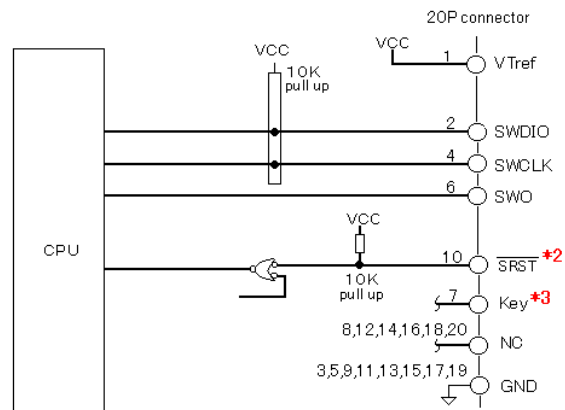
\*3: "Key" is intended for protection against wrong insertion.

- This interface does not use TRST.

If the target CPU presents a pin specifically for TRST, pull it up with 10K ohmic value.

- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

#### Target connection reference diagram



### 4 SWD interface + Trace

#### Signals

Pin No.	Signal	Input/Output <sup>*1</sup>	Pin No.	Signal	Input/Output <sup>*1</sup>
1	Vtref	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO <sup>*2</sup>	Output
7	Key <sup>*5</sup>		8	NC	
9	GND		10	SRST <sup>*3</sup>	Input
11	GND		12	TraceClk	Output
13	GND		14	TraceD0/SWO <sup>*4</sup>	Output
15	GND		16	TraceD1	Output
17	GND		18	TraceD2	Output
19	GND		20	TraceD3	Output

\*1: Input/output is based on the target system.

\*2: Connect the signal dedicated to SWO. The pin can be left N.C. if you are using Pin No. 14 as SWO (See \*4).

\*3: SRST signal is an open-collector output. Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.

\*4: In some CPUs, SWO and TraceD0 are multiplexed. In the case of such pin, connect SWO signal not to Pin No. 6 but to Pin No.14 even when you intend to use Pin No. 14 as SWO, not as TraceD0.

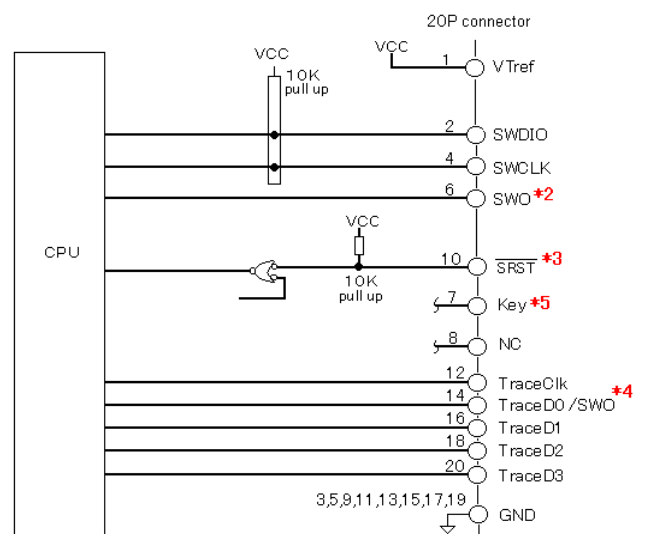
\*5: "Key" is intended for protection against wrong insertion.

- This interface does not use TRST.

If the target CPU presents a pin specifically for TRST, pull it up with 10K ohmic value.

- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

#### Target connection reference diagram



## 5 JTAG interface + Trace

### Signals

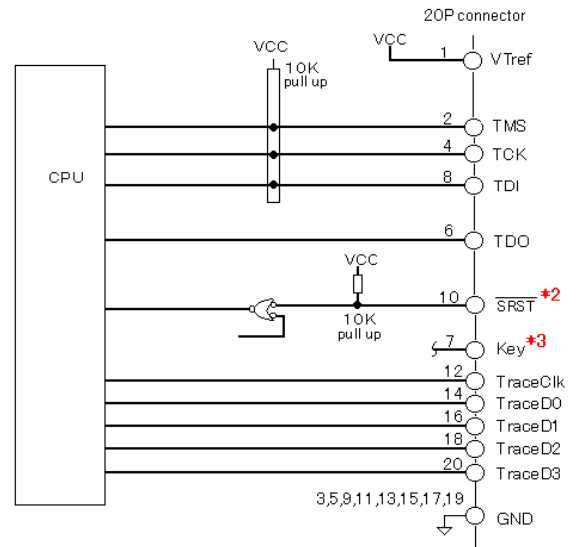
Pin No.	Signal	Input/Output <sup>*1</sup>	Pin No.	Signal	Input/Output <sup>*1</sup>
1	Vtref	Output	2	TMS	Input/Output
3	GND		4	TCK	Input
5	GND		6	TDO	Output
7	Key <sup>*3</sup>		8	TDI	Input
9	GND		10	$\overline{\text{SRST}}$ <sup>*2</sup>	Input
11	GND		12	TraceClk	Output
13	GND		14	TraceD0	Output
15	GND		16	TraceD1	Output
17	GND		18	TraceD2	Output
19	GND		20	TraceD3	Output

\*1: Input/output is based on the target system.

\*2:  $\overline{\text{SRST}}$  signal is an open-collector output.  
Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.

\*3: "Key" is intended for protection against wrong insertion.

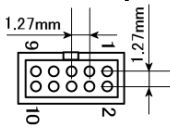
### Target connection reference diagram



- This interface does not use  $\overline{\text{TRST}}$ .  
If the target CPU presents a pin specifically for  $\overline{\text{TRST}}$ , pull it up with 10K ohmic value.
- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.

## 10-pin 1.27mm-pitch connector

### Target connector specifications



(Top view on the target board)

Recommended connector

Manufacturer: Samtec, Inc.

Model: FTSH-105-01-L-DV-K

(For detailed dimensions of the connector, refer to the documentation by manufacturer of the connector.)

## 6 SWD interface

### Signals

Pin No.	Signal	Input/Output <sup>*1</sup>	Pin No.	Signal	Input/Output <sup>*1</sup>
1	VTref	Output	2	SWDIO	Input/Output
3	GND		4	SWCLK	Input
5	GND		6	SWO	Output
7	Key <sup>*3</sup>		8	NC	Input
9	GND		10	SRST <sup>*2</sup>	Input

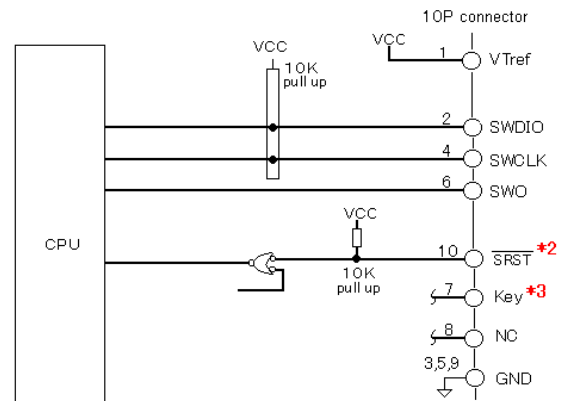
\*1: Input/output is based on the target system.

\*2: SRST signal is an open-collector output.

Establish wired-OR connection to "power-on-reset" or "system reset" on the target system, or if wired-OR circuit is not available, connect with OR circuit.

\*3: "Key" is intended for protection against wrong insertion.

### Target connection reference diagram



- This interface does not use  $\overline{TRST}$ .

If the target CPU presents a pin specifically for  $\overline{TRST}$ , pull it up with 10K ohmic value.

- Keep the length of wirings from CPU to the target connector as short as possible. If the length gets long, it could possibly be a factor contributing to malfunction.