

PALMiCE3 JTAG emulator

PALMiCE3 SH7055



PALMiCE3-SH7055 is a JTAG emulator that incorporates on-chip debugging function in SH-2E core CPUs SH7055F/55SF/58F/58SF/59F. The host interface supports USB2.0(High-speed) to allow faster processing of various tasks such as high-speed downloading. Yet, the Vbus, which requires no power supply, is also supported in PALMiCE3-SH7055 as the feature was well received in PALMiCE2. Note that this product is different from those for other CPUs of SuperH family in that it imposes restrictions due to the specification which makes the debug monitor always resident in memory space of the user, however, it is powerful for debugging of the target you prefer to avoid break thanks to real-time RAM monitor feature support which allows referencing/editing of the target memory and I/O during the user program execution. As for the debugger, it surely incorporates CSIDE, which provides a user-friendly debugging environment. CSIDE supports not only high-level language debugging of a range of C languages but also fully prepared for the debugging of a range of RTOSs with optional debug libraries.

- Supports USB2.0(High-speed), allowing high-speed processing
- A palm-sized, compact body
- Supports on-chip flash memory
- Comes with on-chip flash memory downloader
- Real-time RAM monitor feature
- Requires no power supply with Vbus support
- CPU break and branch tracing features
- Supports SuperH family (Optional)
- Supports debugging of a range of RTOSs (Optional)

Main Specifications

Supported CPUs	SH-2E core CPUs	SH7055F(40MHz), SH7055SF(40MHz), SH7058F(80MHz), SH7058SF(80MHz), SH7059F(80MHz)	
Target I/F	Voltage	Output: 1.2V - 3.6V (Follows target) or fixed to 3.3V Input: 5V-tolerant	
	Voltage measurement	Measures by sampling and shows the results with accuracy of 50mV and precision showing 2 decimal places.	
	Connector	36-pin MDR connector, 40cm cable	
H-UDI clock		Can be set freely in 0.5MHz increments between 1MHz and 20MHz.	
Register, memory, I/O operation		Allows referencing/editing of register, referencing of memory and I/O. (During the user program execution, referencing of memory and I/O can be implemented by Real-time RAM monitor feature.)	
On-chip flash memory support		Supports software break settings and ordinary memory rewriting feature in addition to downloading.	
Debug monitor *1		SH7055F/55SF/58F/58SF does not house the memory dedicated to the debug monitor. The debug monitor occupies the target memory (Occupies Code=5.8K bytes, Data=350 bytes, Stack=48 bytes). Downloading to on-chip flash memory is to be done by connecting RS-232C port of the host computer with SCI port of CPU, and then by running Flash Memory Downloader accompanying CSIDE. Once the monitor program is downloaded, downloading to on-chip flash memory and editing of memory can be implemented directly from CSIDE.	
Software break feature		Supports up to 256 points with instruction replacement method.	
CPU break feature		Occupies UBC and it can be set for 1 point (Before instruction execution / data access / each cycle in DMA access / address mask option / data mask option can be specified.)	
Branch tracing feature	Tracing memory	512K cycle(with 28-bit time stamp)	
	Trace clock	1/2 of CPU clock	
	Reading	Shows branching destination.	
Real-time RAM monitor feature		Allows referencing/editing of CPU on-chip memory, I/O, and the target memory during the user program execution. It is perfect for the target debugging that pursues realtimeliness. (This feature and Branch tracing feature cannot be used at the same time.)	
Reset feature		Debugger can be started up in synchronization with the target by clipping the RESET probe to power-on-reset circuit in the target.	
Execution time measurement		Measures execution time of the user program (64-bit counter, measurement unit=50ns)	
Undo Trace into feature		Feature to virtually go back in Trace into execution (Single-step execution)	
Debugger included as standard		CSIDE for PALMiCE3 SH7055-E	
General specifications	Power specification	DC+5V 350mA (Vbus support for USB)	
	Outside dimensions	95mm(W) x70mm (D) x21mm (H)	
	Host I/F	USB mini-B connector	
	Operating environment	Host computer	The computers running on the supported OSs
		CD drive	Required at the time of installation
		USB	USB2.0
OS	Windows 2000 (Service Pack 4 onward) / Windows XP 32-bit version (Service Pack 1 onward) / Windows Vista 32-bit version / Windows 7 32-bit version, 64-bit version		
Product components		PALMiCE3 AUD360 model main unit set / 2m USB cable / dedicated debugger (CD-ROM)	
Support System		Yes	

*1: You need to customize the debug monitor program to make it suitable for the user system.

Note that the provided debug monitor source is described in Renesas C. To use other compilers, You need to change the monitor source to the specification that can be compiled.

Supported languages

Supported compiler	Renesas C
Supported RTOS	HI7000, HI7000/4, NORTi, osCAN SH2 (Requires optional debug libraries dedicated to each RTOSs.)

* : For details on supported versions, please contact us.

Optional CSIDE

Product name	Description
CSIDE for PALMiCE3 SH-E	Optional CSIDE for debugging of SuperH family CPUs other than SH7055 series.

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