



FPGA + CPU emulator

# F-Sight 2VP-PPC

specifically for Xilinx-made FPGA hard-core processor "PowerPC"



F-Sight 2VP-PPC is an emulator dedicated to Xilinx-made Virtex-II Pro / Virtex-4 FX / Virtex-5 FXT FPGAs embedded with "PowerPC" microprocessors. F-Sight has both functionalities of JTAG emulator with PowerPC software debugging capability and of the analyzer with FPGA hardware debugging capability. These capabilities work in interlock to realize cooperative debugging on the live target. Not to mention, it allows FPGA configuration.

It realizes simple debugging environment with USB2.0 (high-speed support) interface for connection to the host PC and with 38-pin Mictor connector for instant connection to the target system.

As for the debugger software, it incorporates CSIDE, a user-friendly debugging software. It supports high-level language debugging of C languages.

- Supports CPU debugging of PowerPC405 embedded in Virtex-II Pro/Virtex-4 FX and of PowerPC440 embedded in Virtex-5 FXT
- Supports cooperative debugging between CPU (software) and FPGA (hardware)
- 3-in-1 emulator : FPGA debugging / CPU debugging / Cooperative debugging (FPGA + CPU)

- CPU program execution control (Go/Break)
- CPU break feature
- Allows registration of analyzer monitoring signal and automatic wiring from the HDL Source Window (Probing feature)
- Supports JTAG chained devices
- USB 2.0(High-speed) support  
High-speed downloading to target memory  
High-speed configuration
- Supports debugging on flash memory
- Displays program execution log by using CPU tracing feature  
(Realizes the operation in synchronization with Analyzer feature)
- Displays the values of any signals of your choice from the FPGA internal circuits in HDL Source Window (Readback feature)
- Logic analyzer function  
(Realizes the operation in synchronization with CPU tracing feature)
- Easy connections to the host computer and the target system

## Main specifications

Supported devices		Xilinx Virtex-II Pro *1, Virtex-4 FX, Virtex-5 FXT	
Target I/F	FPGA	Pins to be used	FPGA dedicated JTAG interface
		Voltage	2V-3.6V (Automatic adaptation)
		JTAG clock	150KHz, 1MHz, 5MHz, 10MHz, 20MHz or 30MHz to choose from
		Maximum number of devices to be in chain	Up to 8 (The total sum of JTAG instruction lengths must be no larger than 128 bits.)
	CPU *2	Pins to be used	JTAG I/F : FPGA pins dedicated to JTAG or I/O pins CPU tracing :Assigns I/O pins with CPU tracing signals
		Voltage	1.2V-3.6V (Automatic adaptation)
		JTAG clock	1MHz - 40MHz
	Current consumption	50uA or less	
	Voltage measurement	Measures by sampling and shows the results with accuracy of 50mV and precision showing 2 decimal places.	
	Connector	38-pin Mictor connector	
FPGA functionality *3	Supported tools *4	Xilinx-made ISE 8.1i/EDK 8.1i ISE 8.2i/EDK 8.2i ISE 9.1i/EDK 9.1i ISE 9.2i/EDK 9.2i ISE 10.1i/EDK 10.1i ISE 11.1i/EDK 11.1i ISE 11.2i/EDK 11.2i ISE 11.3i/EDK 11.3i ISE 11.4i/EDK 11.4i ISE 11.5i/EDK 11.5i	
	Supported languages	VHDL, Verilog	
	Probing feature	Automatically routes FPGA internal nodes to FPGA pins in wiring.	
	Readback feature *5	Displays internal nodes and block RAM contents by sampling.	
CPU functionality	Linkage feature	Loads ISE in the background and automatically executes from synthesis through configuration.	
	Execution control	Program execution, Break, Step execution, Trace execution, Come execution	
	Register, memory operation	Supports referencing/editing of register and memory and downloading to memory during break.	
	Software break	256 points	
	CPU break	For programs: 4 points; for data: 2 points.	
	Flash memory support	In addition to downloading to a range of flash memories, it also supports debugging features such as software break settings and ordinary memory rewriting feature. Also, new device can be added easily through GUI.	
Analyzer feature	Execution time measurement	Measures execution time of the user program (64-bit counter, measurement unit=1uS)	
	Capacity	512K cycles	
	Sampling clock	Max. 200MHz	
	Input voltage	0V~3.6V	
	Threshold voltage settings	Can be specified between 0.3 V and 2.2 V in 0.1 V increment.	
	Trigger settings	CPU event, Analyzer pattern condition, Edge option	
	Trigger position	Any of 5 positions between START and END can be specified.	
	Trigger mode	Trigger stop, Trigger break	
Number of channels	PowerPC405	16 channels (8 channels of which are for CPU tracing) as standard plus 32 channels for optional expansion	
	PowerPC440	16 channels (15 channels of which are for CPU tracing) as standard plus 32 channels for optional expansion	
	Time stamping feature	10nS or 1uS to choose from	

\*1: XC2VP2 and Virtex-II Pro X are not supported. \*2: Can be connected in chain with JTAG I/F specifically for FPGA.

\*3: To use FPGA features, in order to implement FPGA functionality, ISE needs to be installed on the computer you use.

\*4: For the state of support provision for the latest version of service pack, please contact us.

\*5: The FPGA ceases operation (shuts down) when readback feature is used.

**Main specifications**

<b>General specifications</b>	<b>Standard debugger</b>		CSIDE for F-Sight 2VP-PPC-E	
	Current consumption		DC+5V, Approx. 2.5A max.	
	Dedicated AC adapter		Input: AC100V to 240V, Output: 5V, 3.5A	
	Outside dimensions		106mm (W) x 78mm (D) x 29.5mm (H)	
	Host I/F		USB mini-B (5-pin) connector	
	Operating environment *6	Host computer	The computers running on the supported OSs	
		CD drive	Required at the time of installation	
		USB	USB2.0	
OS		Windows 2000 / Windows XP / Windows Vista / Windows 7		
<b>Support System</b>			Available	

\*6: If you wish to use FPGA functionality, do observe the recommended operating environment for Xilinx-made ISE.

**Supported languages**

Supported C compiler	GNU C accompanying Platform studio
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Note: For details on supported languages and supported versions, please contact us.

**Other optional products**

Product name	Description
FS-EXANZ32	Probe for adding 32 more channels to analyzer.
FS-ADP-SEPA	Conversion adapter set for the target systems not prepared with a Mictor connector.
FS-ADP-ML403	Conversion adapter specifically for Xilinx-made ML403/ML405/ML501/ML507 board.
ADP-FS-2VP-SUZAKU-V	Conversion adapter specifically for Atmark Techno-made SUZAKU Starter Kit



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